Understanding power supply ripple rejection in linear regulators

By John C. Teel (Email: jteel@ti.com)

Analog IC Designer, Member Group Technical Staff

Power supply ripple rejection ratio (PSRR) is a measure of how well a circuit rejects ripple coming from the input power supply at various frequencies and is very critical in many RF and wireless applications. In the case of an LDO, it is a measure of the output ripple compared to the input ripple over a wide frequency range (10 Hz to 10 MHz is common) and is expressed in decibels (dB). The basic equation for PSRR is

$$\mathrm{PSRR} = 20\log\frac{\mathrm{Ripple}_{\mathrm{Input}}}{\mathrm{Ripple}_{\mathrm{Output}}}.$$

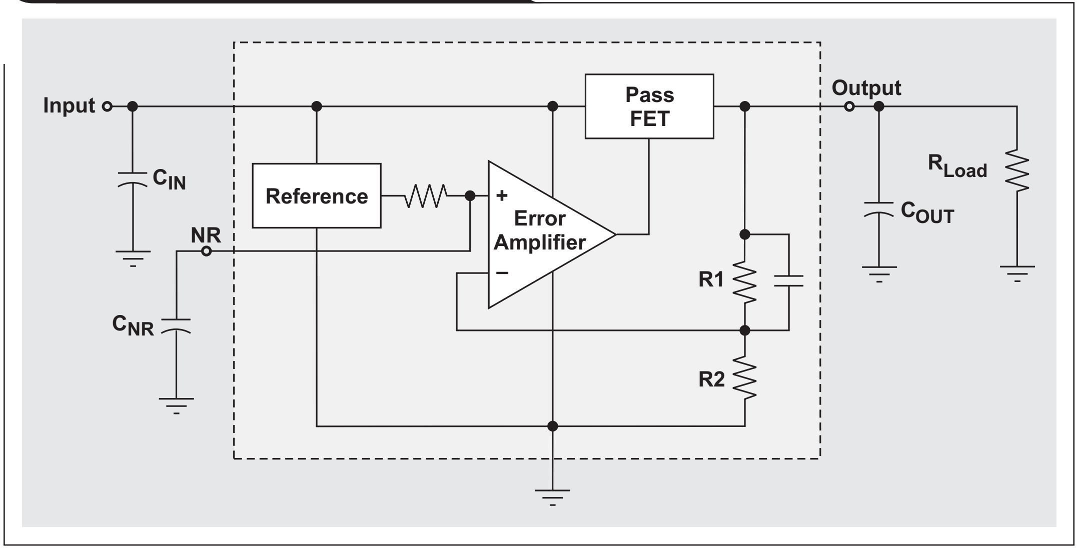
More specifically, PSRR for an LDO can be written as

$$\mathrm{PSRR} = 20\log\frac{A_V}{A_{VO}},$$

where A_V is the open-loop gain of the regulator feedback loop, and A_{VO} is the gain from V_{IN} to V_{OUT} with the regulator feedback loop open. From this equation it can be seen that to increase the PSRR it is beneficial to increase the open-loop gain and decrease the gain from V_{IN} to V_{OUT}. Typically, A_{VO} is significantly less than 0 dB, with –10 to –15 dB being typical; this is entirely driven by internal and external parasitics from input to output and at the gate of the pass FET. Figure 1 shows a simplified regulator block diagram with a PMOS pass device.

Another parameter that is closely related to PSRR is line transient response. PSRR is specified at specific frequencies, whereas a line transient essentially contains all frequencies due to the Fourier components of a step function. However, the primary difference is that PSRR is based on small signals, whereas line transients are large signals and thus theoretically much more complicated in nature. Since improving PSRR typically improves line transient response and vice versa, all of the effects on PSRR discussed in this article will usually have a similar effect on the line transient response.

Figure 1. Simplified LDO block diagram



A curve showing PSRR over a wide frequency range is shown in Figure 2.

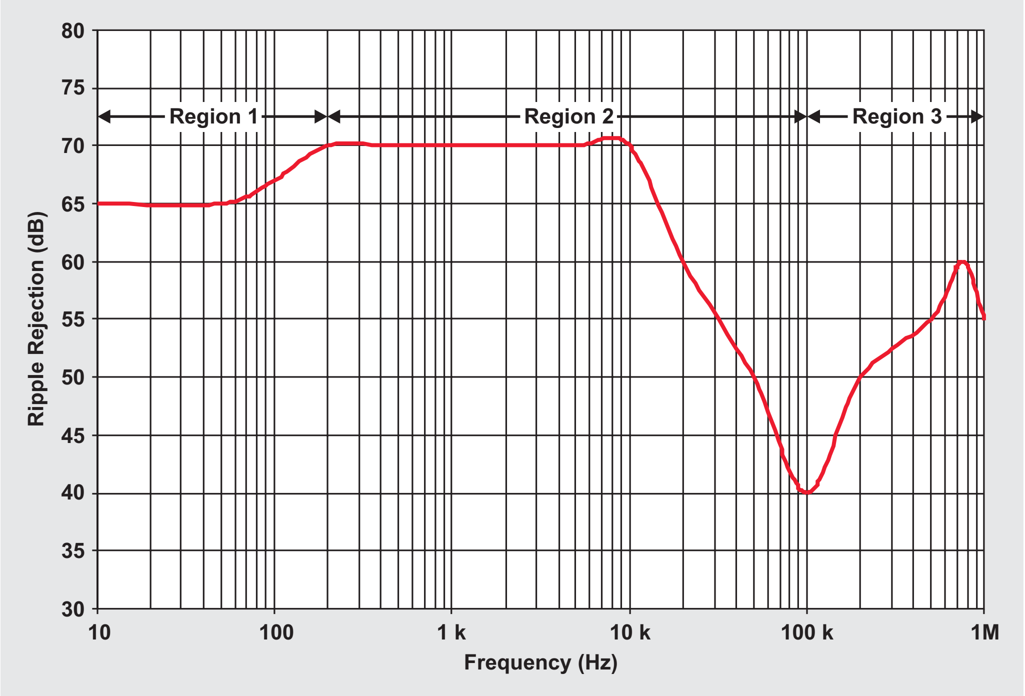
As mentioned previously, the open-loop gain of the LDO feedback circuit is the dominant factor in PSRR (at least in a limited frequency range); therefore, LDOs requiring good PSRR typically have high gain with a high unity-gain frequency (large gain-bandwidth product). However, this makes the loop more difficult to stabilize, which limits how much the gain-bandwidth product can be increased to improve PSRR. It is important to have a high unity-gain frequency so that the amplifier does not lose open-loop gain at relatively low frequencies, causing PSRR to roll off also.

The curve in Figure 2 shows that PSRR for an LDO can be broken down into three basic frequency regions. Region 1 is from dc to the roll-off frequency of the bandgap filter and is dominated by both open-loop gain and bandgap PSRR. Region 2 extends from the bandgap filter roll-off frequency up to the unity-gain frequency where PSRR is dominated mainly by the open-loop gain of the regulator. Region 3 is above the unity-gain frequency, where the feedback loop has very little effect, so the output capacitor dominates along with any parasitics from V_{IN} to V_{OUT}. The gate driver's ability to drive the pass-FET gate at high frequencies also has an effect in Region 3. A larger output capacitor with less equivalent series resistance (ESR) will typically improve PSRR in this region, but it can also actually decrease the PSRR at some frequencies. This is because increasing the output capacitor lowers the unity-gain frequency, causing the open-loop gain to roll off earlier and thus lowering PSRR. Nevertheless, the minimum PSRR that occurs at the unity-gain frequency will typically be improved.

Anything affecting the gain of the feedback loop also affects PSRR in Region 2. One example is load current. As load current increases, the open-loop output impedance of the LDO decreases (since a MOSFET's output impedance is inversely proportional to the drain current), thus lowering the gain. Increasing the load current also pushes the output pole to higher frequencies, which increases the feedback loop bandwidth.The net effect of increasing the load is therefore reduced PSRR at lower frequencies (because of the reduced gain) along with increased PSRR at higher frequencies.

The differential dc voltage between input and output is another example of how a change in the feedback loop gain also affects PSRR. As $V_{IN}–V_{OUT}$ is lowered to less than about 1 V, the internal pass FET (which provides gain in a PMOS design) starts to be pushed out of the active (saturation) region of operation and into the triode/linear region, which causes the feedback loop to lose gain. The dividing line between the active region and the triode region is proportional to the square root of the drain (load) current. So as the load current is increased, the voltage across the device ($V_{IN}–V_{OUT}$) necessary to keep it in the active region increases as a function of the square root of the load current. For example, having $V_{IN}–V_{OUT}$ at only 0.5 V may have no negative effect on PSRR at light load currents because the pass FET device doesn't need much headroom to stay in the active region and to preserve gain. At heavier loads,

Figure 2. PSRR curve



however, 0.5 V may no longer be sufficient and the pass FET device may enter the triode region, causing the circuit to lose gain, thus reducing PSRR. When PSRR is compared among various LDOs, it's important always to compare LDOs with identical $V_{IN}–V_{OUT}$ and I_{Load} conditions. It's also important to compare LDOs with identical output voltages, since PSRR is usually better at lower output voltages.

One of the dominant internal sources of PSRR in an LDO is the bandgap reference. Any ripple that makes its way onto the reference will be amplified and sent to the output, so it's important to have a bandgap reference with high PSRR. Typically, the solution is simply to filter the bandgap with a low-pass filter (LPF). This LPF is almost always accomplished with a large internal resistor and an external capacitor. The effect of the LPF can be seen in Region 1 of Figure 2, where the PSRR is somewhat reduced because the LPF passes bandgap ripple in this frequency range.

As has been shown, there are many ways to improve the PSRR in an LDO application. The most important is to start with a low-noise, high-PSRR LDO designed for high-PSRR applications such as one from the TPS793/4/5/6xx family or the low-I_q TPS799xx family. The next most important way is to choose a low-ESR ceramic output capacitor and to determine the capacitance value based on the frequencies at which PSRR is most important. Finally, board layout must be carefully done to reduce the feedthrough from input to output via board parasitics.

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