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24-Channel, 12-Bit PWM LED Driver with Internal Oscillator

FEATURES

- 24 Channels, Constant Current Sink Output
- 30-mA Capability (Constant Current Sink)
- 12-Bit (4096 Steps) PWM Grayscale Control
- LED Power-Supply Voltage up to 30 V
- V_{CC} = 3.0 V to 5.5 V
- Constant Current Accuracy:
  - Channel-to-Channel = ±2% (typ)
  - Device-to-Device = ±2% (typ)
- CMOS Logic Level I/O
- 30-MHz Data Transfer Rate (Standalone)
- 15-MHz Data Transfer Rate (Cascaded Devices, SCLK Duty = 50%)
- Shift Out Data Changes With Falling Edge to Avoid Data Shift Errors
- Auto Display Repeat
- 4-MHz Internal Oscillator
- Thermal Shutdown (TSD):
  - Automatic shutdown at over temperature conditions
  - Restart under normal temperature
- Noise Reduction:
  - 4-channel grouped delay to prevent inrush current
- Operating Temperature: –40℃ to +85℃

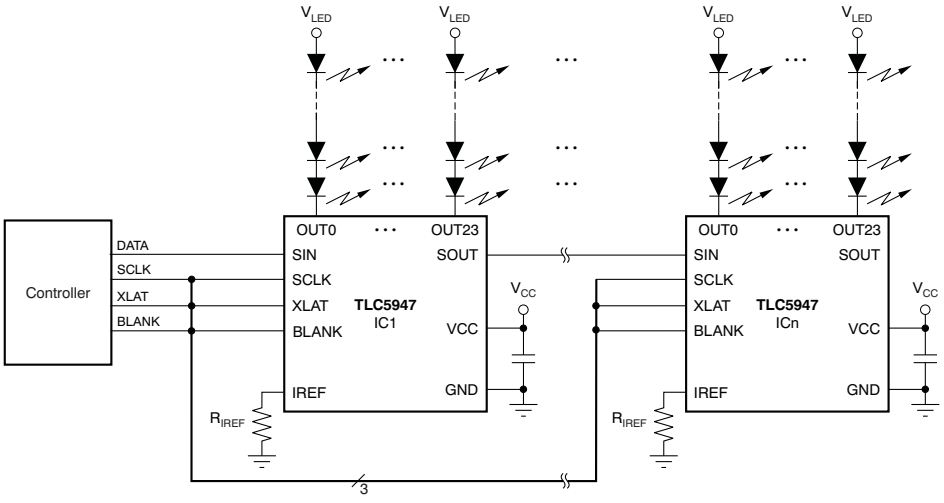
APPLICATIONS

- Static LED Displays
- Message Boards
- Amusement Illumination
- TV Backlighting

DESCRIPTION

The TLC5947 is a 24-channel, constant current sink LED driver. Each channel is individually adjustable with 4096 pulse-width modulated (PWM) steps. PWM control is repeated automatically with the programmed grayscale (GS) data. GS data are written via a serial interface port. The current value of all 24 channels is set by a single external resistor.

The TLC5947 has a thermal shutdown (TSD) function that turns off all output drivers during an over-temperature condition. All of the output drivers automatically restart when the temperature returns to normal conditions.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLC5947	HTSSOP-32 PowerPAD™	TLC5947DAPR	Tape and Reel, 2000
		TLC5947DAP	Tube, 46
TLC5947	5-mm × 5-mm QFN-32	TLC5947RHBR	Tape and Reel, 3000
		TLC5947RHB	Tape and Reel, 250

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Over operating free-air temperature range, unless otherwise noted.

PARAMETER			TLC5947	UNIT
V_{CC}	Supply voltage: V_{CC}		–0.3 to +6.0	V
I_O	Output current (dc)	OUT0 to OUT23	38	mA
V_I	Input voltage range	SIN, SCLK, XLAT, BLANK	–0.3 to V_{CC} + 0.3	V
V_O	Output voltage range	SOUT	–0.3 to V_{CC} + 0.3	V
		OUT0 to OUT23	–0.3 to +33	V
$T_{J(MAX)}$	Operating junction temperature		+150	℃
T_{STG}	Storage temperature range		–55 to +150	℃
	ESD rating	Human body model (HBM)	2	kV
		Charged device model (CDM)	500	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS

PACKAGE	OPERATING FACTOR ABOVE T_A = +25℃	T_A < +25℃ POWER RATING	T_A = +70℃ POWER RATING	T_A = +85℃ POWER RATING
HTSSOP-32 with PowerPAD soldered(1)	42.54 mW/℃	5318 mW	3403 mW	2765 mW
HTSSOP-32 with PowerPAD not soldered(2)	22.56 mW/℃	2820 mW	1805 mW	1466 mW
QFN-32(3)	27.86 mW/℃	3482 mW	2228 mW	1811 mW

(1) With PowerPAD soldered onto copper area on printed circuit board (PCB); 2 oz. copper. For more information, see SLMA002 (available for download at www.ti.com).
(2) With PowerPAD not soldered onto copper area on PCB.
(3) The package thermal impedance is calculated in accordance with JESD51-5.

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RECOMMENDED OPERATING CONDITIONS

At T_A= –40℃ to +85℃, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5947			UNIT
			MIN	NOM	MAX	
DC Characteristics: V_{CC} = 3 V to 5.5 V						
V_{CC}	Supply voltage		3.0		5.5	V
V_O	Voltage applied to output	OUT0 to OUT23			30	V
V_{IH}	High-level input voltage		0.7 × V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage		GND		0.3 × V_{CC}	V
I_{OH}	High-level output current	SOUT			–3	mA
I_{OL}	Low-level output current	SOUT			3	mA
I_{OLC}	Constant output sink current	OUT0 to OUT23	2		30	mA
T_A	Operating free-air temperature range		–40		+85	℃
T_J	Operating junction temperature		–40		+125	℃
AC Characteristics: V_{CC} = 3 V to 5.5 V						
f_{SCLK}	Data shift clock frequency	SCLK, Standalone operation			30	MHz
		SCLK, Duty 50%, cascade operation			15	MHz
T_{WH0}	Pulse duration	SCLK = High-level pulse width	12			ns
T_{WL0}		SCLK = Low-level pulse width	10			ns
T_{WH1}		XLAT, BLANK High-level pulse width	30			ns
T_{SU0}	Setup time	SIN–SCLK↑	5			ns
T_{SU1}		XLAT↑–SCLK↑	100			ns
T_{SU2}		XLAT↑–BLANK↓	30			ns
T_{H0}	Hold time	SIN–SCLK↑	3			ns
T_{H1}		XLAT↑–SCLK↑	10			ns

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ELECTRICAL CHARACTERISTICS

At V_{CC} = 3.0 V to 5.5 V and T_A = –40°C to +85°C. Typical values at V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5947			UNIT
			MIN	TYP	MAX	
V_{OH}	High-level output voltage	I_{OH} = –3 mA at SOUT	V_{CC} – 0.4		V_{CC}	V
V_{OL}	Low-level output voltage	I_{OL} = 3 mA at SOUT			0.4	V
I_{IN}	Input current	V_{IN} = V_{CC} or GND at SIN, XLAT, and BLANK	–1		1	µA
I_{CC1}	Supply current (V_{CC})	SIN/SCLK/XLAT = low, BLANK = high, V_{OUTn} = 1 V, R_{IREF} = 24 kΩ		0.5	3	mA
I_{CC2}		SIN/SCLK/XLAT = low, BLANK = high, V_{OUTn} = 1 V, R_{IREF} = 3.3 kΩ		1	6	mA
I_{CC3}		SIN/SCLK/XLAT = low, BLANK = low, V_{OUTn} = 1 V, R_{IREF} = 3.3 kΩ, GSn = FFFh		15	45	mA
I_{CC4}		SIN/SCLK/XLAT = low, BLANK = low, V_{OUTn} = 1 V, R_{IREF} = 1.6 kΩ, GSn = FFFh		30	90	mA
I_{OLC}	Constant output current	All OUTn = ON, V_{OUTn} = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 1.6 kΩ	27.7	30.75	33.8	mA
I_{OLK}	Output leakage current	BLANK = high, V_{OUTn} = 30 V, R_{IREF} = 1.6 kΩ, At OUT0 to OUT23			0.1	µA
ΔI_{OLC}	Constant current error (channel-to-channel)(1)	All OUTn = ON, V_{OUTn} = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 1.6 kΩ, At OUT0 to OUT23		±2	±4	%
ΔI_{OLC1}	Constant current error (device-to-device)(2)	All OUTn = ON, V_{OUTn} = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 1.6 kΩ		±2	±7	%
ΔI_{OLC2}	Line regulation(3)	All OUTn = ON, V_{OUTn} = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 1.6 kΩ, At OUT0 to OUT23		±1	±3	%/V
ΔI_{OLC3}	Load regulation(4)	All OUTn = ON, V_{OUTn} = 1 V to 3 V, V_{OUTfix} = 1 V, R_{IREF} = 1.6 kΩ, At OUT0 to OUT23		±2	±6	%/V
T_{DOWN}	Thermal shutdown threshold	Junction temperature(5)	+150	+162	+175	°C
T_{HYS}	Thermal error hysteresis	Junction temperature(5)	+5	+10	+20	°C
V_{IREF}	Reference voltage output	R_{IREF} = 1.6 kΩ	1.16	1.20	1.24	V

(1) The deviation of each output from the average of OUT0–OUT23 constant current. Deviation is calculated by the formula:

$$\Delta\ (\%) = \left(\frac{I_{OUTn}}{\frac{(I_{OUT0} + I_{OUT1} + \ldots + I_{OUT22} + I_{OUT23})}{24}} - 1 \right) \times 100$$

(2) The deviation of the OUT0–OUT23 constant current average from the ideal constant current value. Deviation is calculated by the following formula:

$$\Delta\ (\%) = \left(\frac{\frac{(I_{OUT0} + I_{OUT1} + \ldots I_{OUT22} + I_{OUT23})}{24} - (\text{Ideal Output Current})}{\text{Ideal Output Current}} \right) \times 100$$

Ideal current is calculated by the formula:

$$I_{OUT(IDEAL)} = 41 \times \left(\frac{1.20}{R_{IREF}} \right)$$

(3) Line regulation is calculated by this equation:

$$\Delta\ (\%/V) = \left(\frac{(I_{OUTn} \text{ at } V_{CC} = 5.5\ V) - (I_{OUTn} \text{ at } V_{CC} = 3.0\ V)}{(I_{OUTn} \text{ at } V_{CC} = 3.0\ V)} \right) \times \frac{100}{5.5\ V - 3\ V}$$

(4) Load regulation is calculated by the equation:

$$\Delta\ (\%/V) = \left(\frac{(I_{OUTn} \text{ at } V_{OUTn} = 3\ V) - (I_{OUTn} \text{ at } V_{OUTn} = 1\ V)}{(I_{OUTn} \text{ at } V_{OUTn} = 1\ V)} \right) \times \frac{100}{3\ V - 1\ V}$$

(5) Not tested. Specified by design.

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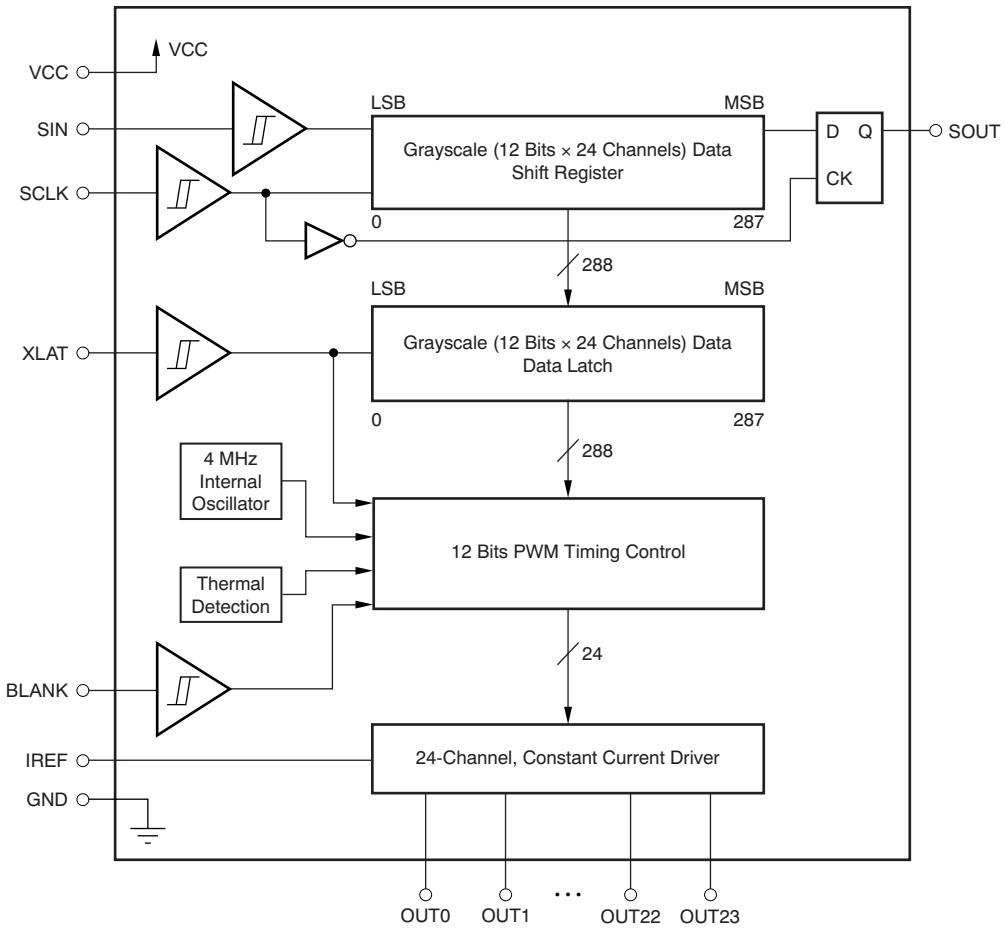
SWITCHING CHARACTERISTICS

At V_{CC} = 3.0 V to 5.5 V, T_A = –40℃ to +85℃, C_L = 15 pF, R_L = 150 Ω, R_{IREF} = 1.6 kΩ, and V_{LED} = 5.5 V. Typical values at V_{CC} = 3.3 V and T_A = +25℃, unless otherwise noted.

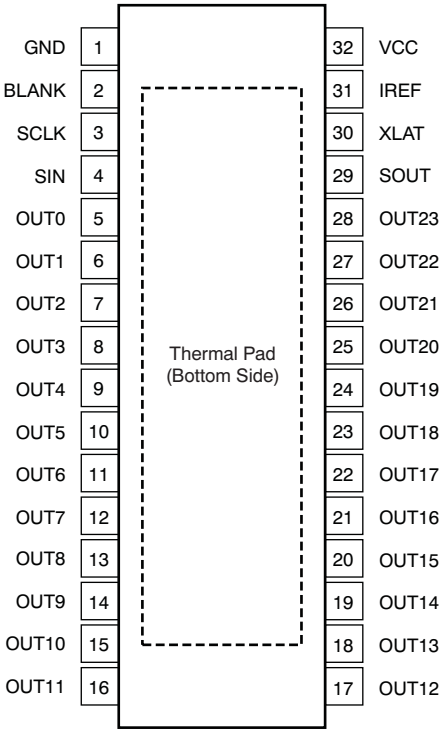
PARAMETER		TEST CONDITIONS	TLC5947			UNIT
			MIN	TYP	MAX	
t_{R0}	Rise time	SOUT		10	15	ns
t_{R1}		OUTn		15	40	ns
t_{F0}	Fall time	SOUT		10	15	ns
t_{F1}		OUTn		100	300	ns
f_{OSC}	Internal oscillator frequency		2.4	4	5.6	MHz
t_{D0}	Propagation delay time	SCLK↓ to SOUT		15	25	ns
t_{D1}		BLANK↑ to OUT0 sink current off		20	40	ns
t_{D2}		OUT0 current on to OUT1/5/9/13/17/21 current on	15	24	33	ns
t_{D3}		OUT0 current on to OUT2/6/10/14/18/22 current on	30	48	66	ns
t_{D4}		OUT0 current on to OUT3/7/11/15/19/23 current on	45	72	99	ns

FUNCTIONAL BLOCK DIAGRAM

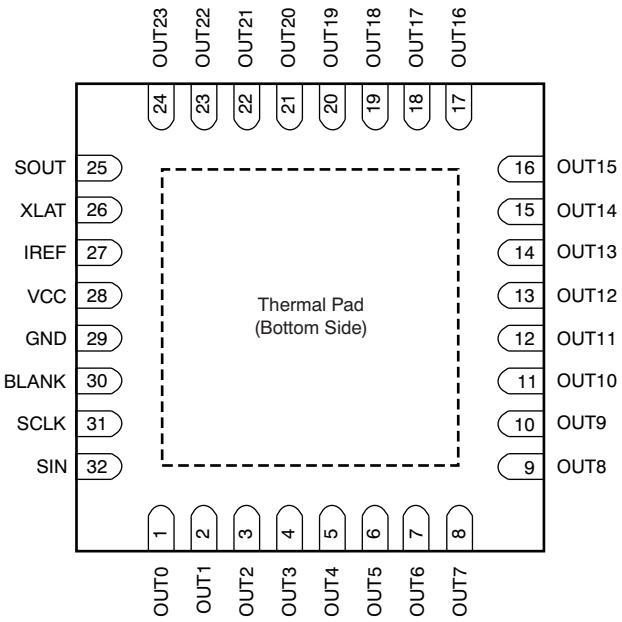


DEVICE INFORMATION

HTSSOP-32
DAP PACKAGE
(TOP VIEW)



5-mm × 5-mm QFN-32(1)
RHB PACKAGE
(TOP VIEW)



(1) This device is product preview.

NOTE: Thermal pad is not connected to GND internally. The thermal pad must be connected to GND via the PCB pattern.

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TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	DAP	RHB		
SIN	4	32	I	Serial input for grayscale data
SCLK	3	31	I	Serial data shift clock. Schmitt buffer input. Data present on the SIN pin are shifted into the shift register with the rising edge of the SCLK pin. Data are shifted to the MSB side by 1-bit synchronizing of the rising edge of SCLK. The MSB data appears on SOUT at the falling edge of SCLK. A rising edge on the SCLK input is allowed 100 ns after an XLAT rising edge.
XLAT	30	26	I	The data in the grayscale shift register are moved to the grayscale data latch with a low-to-high transition on this pin. When the XLAT rising edge is input, all constant current outputs are forced off until the next grayscale display period. The grayscale counter is not reset to zero with a rising edge of XLAT.
BLANK	2	30	I	Blank (all constant current outputs off). When BLANK is high, all constant current outputs (OUT0 through OUT23) are forced off, the grayscale PWM timing controller initializes, and the grayscale counter resets to '0'. When BLANK is low, all constant current outputs are controlled by the grayscale PWM timing controller.
IREF	31	27	I/O	This pin sets the constant current value. OUT0 through OUT23 constant sink current is set to the desired value by connecting an external resistor between IREF and GND.
SOUT	29	25	O	Serial data output. This output is connected to the shift register placed after the MSB of the grayscale shift register. Therefore, the MSB data of the grayscale shift register appears at the falling edge of SCLK. This function reduces the data shifting errors caused by small timing margins between SIN and SCLK.
OUT0	5	1	O	Constant current output. Multiple outputs can be tied together to increase the constant current capability. Different voltages can be applied to each output.
OUT1	6	2	O	Constant current output
OUT2	7	3	O	Constant current output
OUT3	8	4	O	Constant current output
OUT4	9	5	O	Constant current output
OUT5	10	6	O	Constant current output
OUT6	11	7	O	Constant current output
OUT7	12	8	O	Constant current output
OUT8	13	9	O	Constant current output
OUT9	14	10	O	Constant current output
OUT10	15	11	O	Constant current output
OUT11	16	12	O	Constant current output
OUT12	17	13	O	Constant current output
OUT13	18	14	O	Constant current output
OUT14	19	15	O	Constant current output
OUT15	20	16	O	Constant current output
OUT16	21	17	O	Constant current output
OUT17	22	18	O	Constant current output
OUT18	23	19	O	Constant current output
OUT19	24	20	O	Constant current output
OUT20	25	21	O	Constant current output
OUT21	26	22	O	Constant current output
OUT22	27	23	O	Constant current output
OUT23	28	24	O	Constant current output
VCC	32	28	—	Power-supply voltage
GND	1	29	—	Power ground

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PARAMETER MEASUREMENT INFORMATION

PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

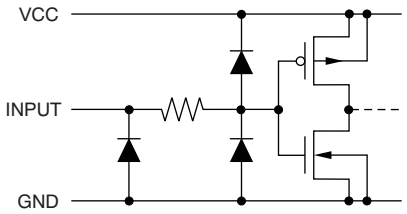

Figure 1. SIN, SCLK, XLAT, BLANK

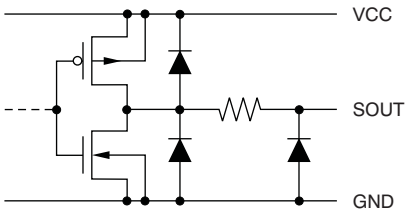

Figure 2. SOUT

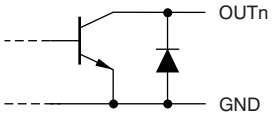

Figure 3. OUT0 Through OUT23

TEST CIRCUITS

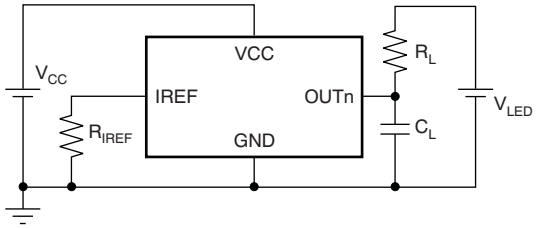

Figure 4. Rise Time and Fall Time Test Circuit for OUTn

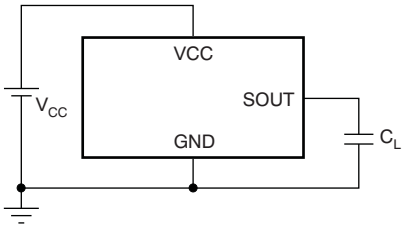

Figure 5. Rise Time and Fall Time Test Circuit for SOUT

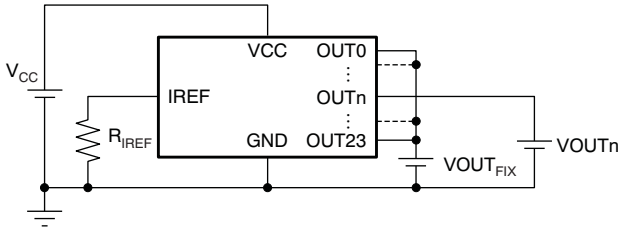

Figure 6. Constant Current Test Circuit for OUTn

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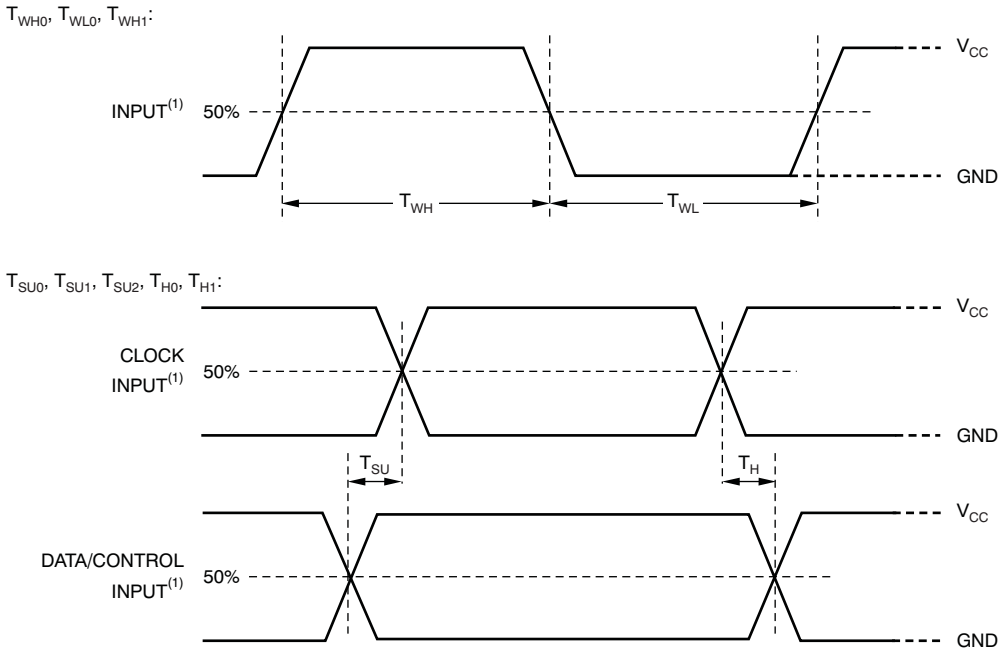
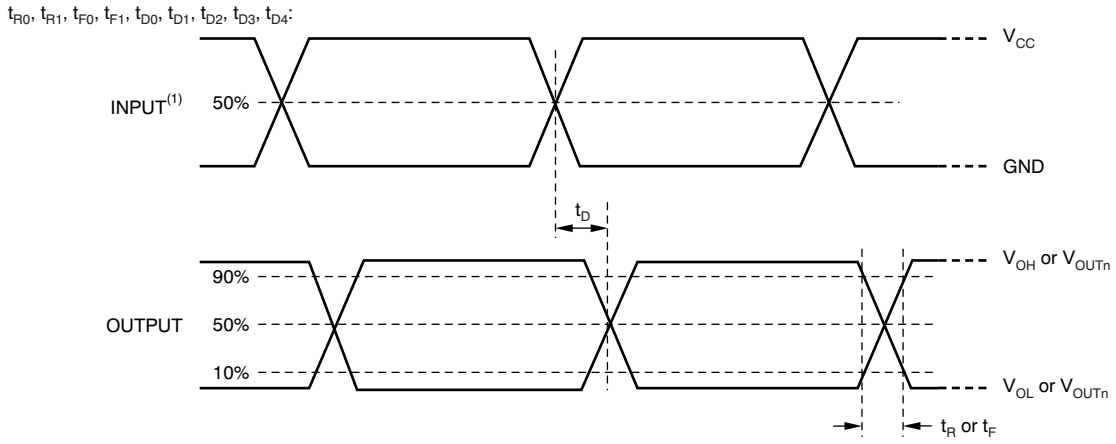
TIMING DIAGRAMS



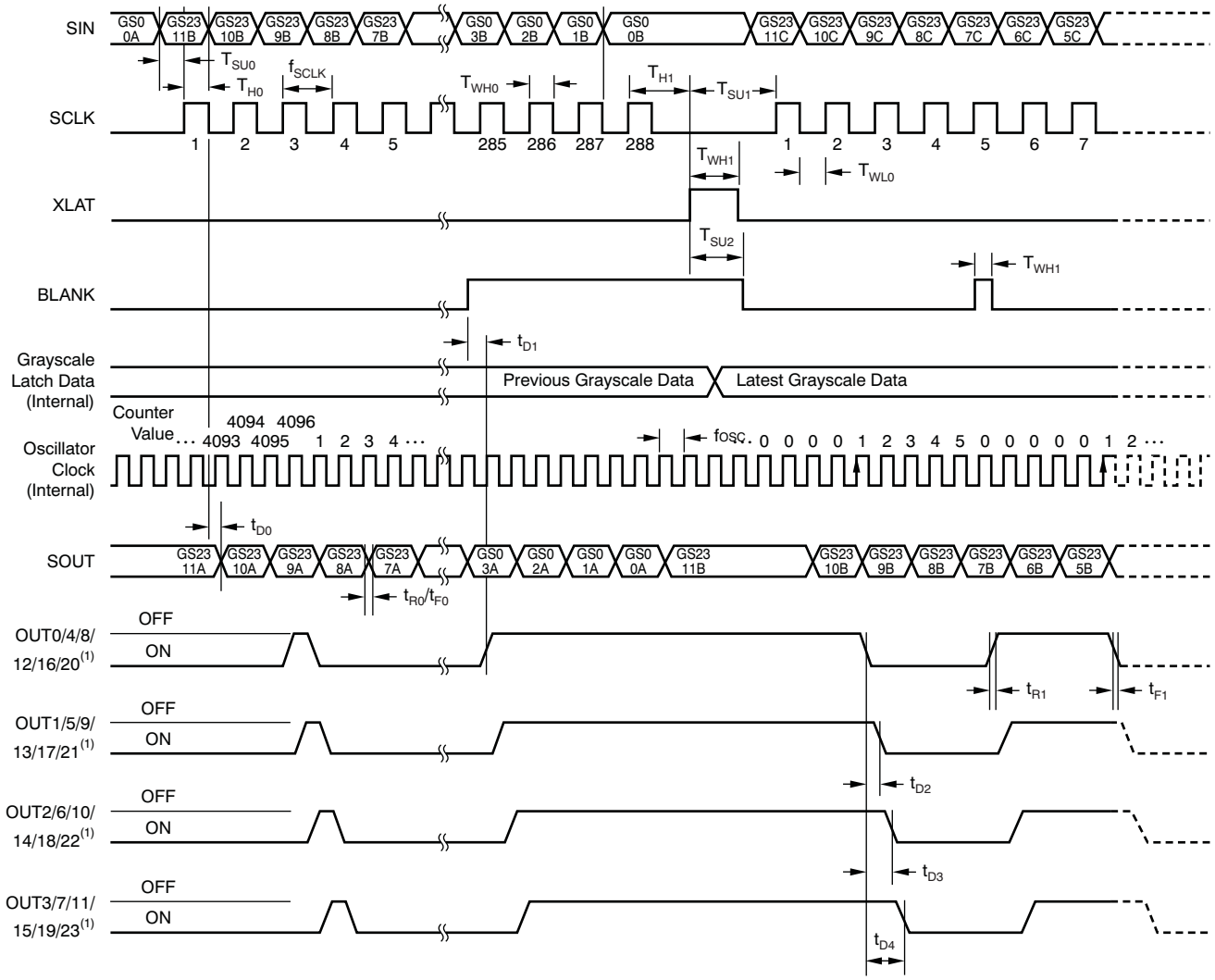
(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 7. Input Timing



(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 8. Output Timing



(1) GS data = FFFh.

Figure 9. Grayscale Data Write and OUTn Operation Timing

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TYPICAL CHARACTERISTICS

At V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

REFERENCE RESISTOR vs OUTPUT CURRENT

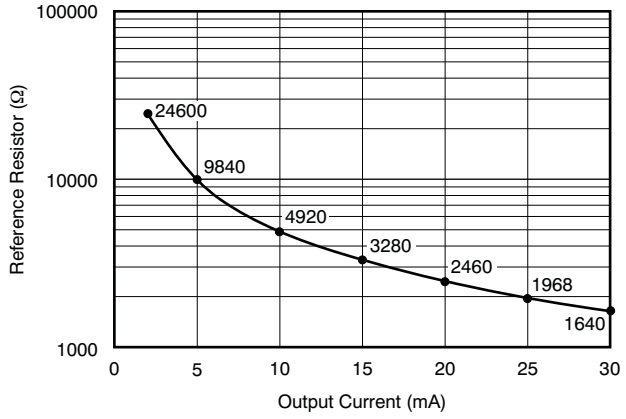

Figure 10.

POWER DISSIPATION RATE vs FREE-AIR TEMPERATURE

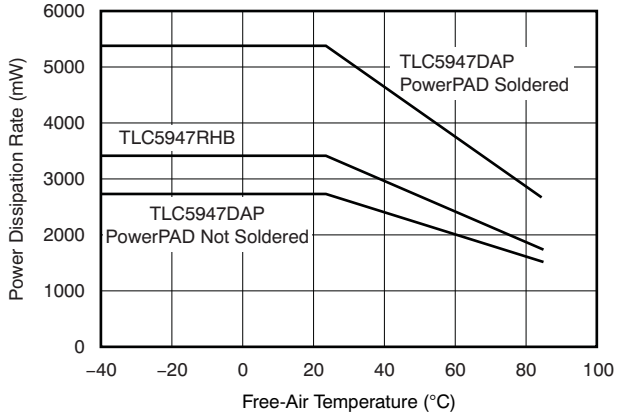

Figure 11.

OUTPUT CURRENT vs OUTPUT VOLTAGE

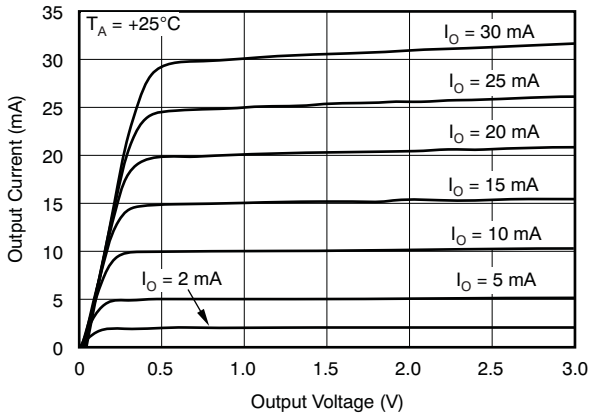

Figure 12.

OUTPUT CURRENT vs OUTPUT VOLTAGE

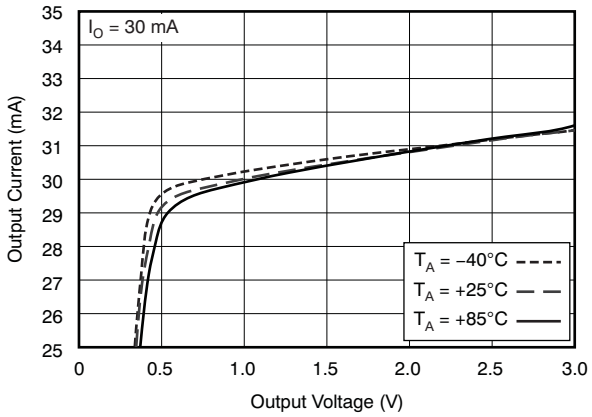

Figure 13.

ΔI_{OLC} vs AMBIENT TEMPERATURE

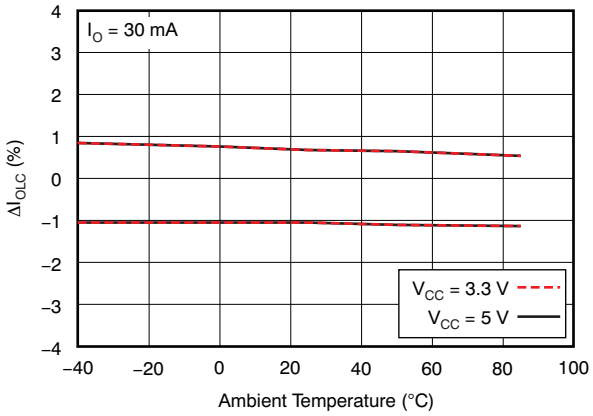

Figure 14.

ΔI_{OLC} vs OUTPUT CURRENT

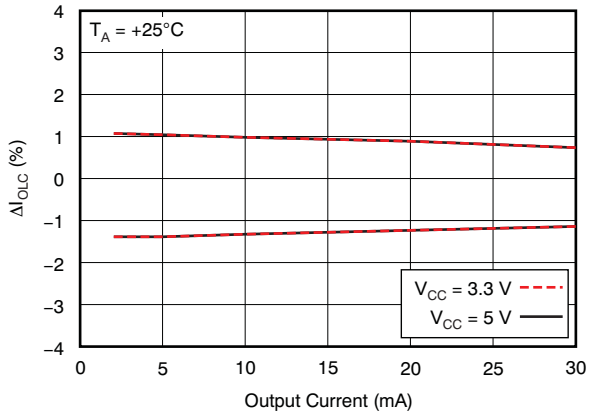

Figure 15.

TYPICAL CHARACTERISTICS (continued)

At V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

INTERNAL OSCILLATOR FREQUENCY vs AMBIENT TEMPERATURE

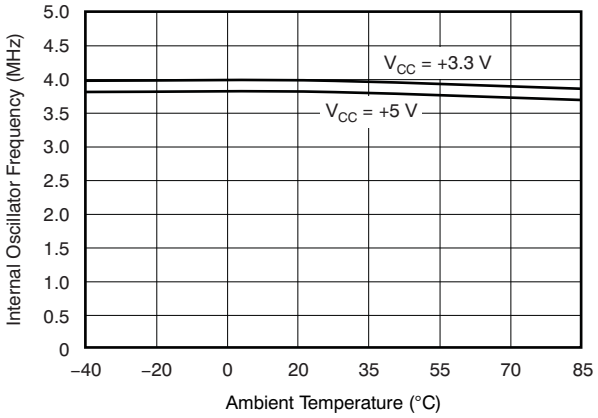

Figure 16.

CONSTANT CURRENT OUTPUT VOLTAGE WAVEFORM

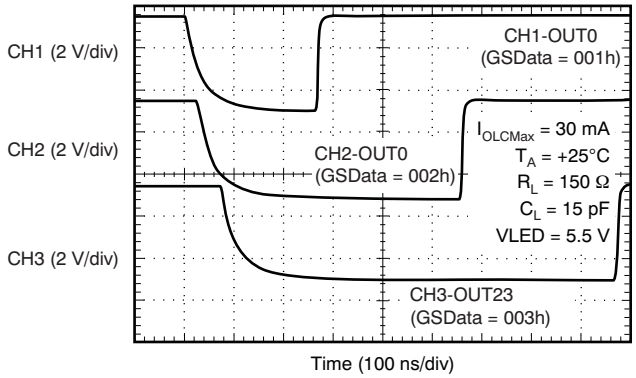

Figure 17.

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DETAILED DESCRIPTION

SETTING FOR THE CONSTANT SINK CURRENT VALUE

The constant current value for all channels is set by an external resistor (R_{IREF}) placed between IREF and GND. The resistor (R_{IREF}) value is calculated by Equation 1.

$$R_{IREF}\ (\Omega) = 41 \times \frac{V_{IREF}\ (V)}{I_{OLC}\ (mA)} \quad (1)$$

Where:

V_{IREF} = the internal reference voltage on the IREF pin (typically 1.20 V).

I_{OLC} must be set in the range of 2 mA to 30 mA. The constant sink current characteristic for the external resistor value is shown in Figure 10. Table 1 describes the constant current output versus external resistor value.

Table 1. Constant-Current Output versus External Resistor Value

I_{OLC} (mA, Typical)	R_{IREF} (Ω)
30	1640
25	1968
20	2460
15	3280
10	4920
5	9840
2	24600

GRAYSCALE (GS) CONTROL FUNCTION

Each constant current sink output OUT0–OUT23 (OUTn) turns on (starts to sink constant current) at the fifth rising edge of the grayscale internal oscillator clock after the BLANK signal transitions from high to low if the grayscale data latched into the grayscale data latch are not zero. After turn-on, the number of rising edges of the internal oscillator is counted by the 12-bit grayscale counter. Each OUTn output is turned off once its corresponding grayscale data values equal the grayscale counter or the counter reaches 4096d (FFFh). The PWM control operation is repeated as long as BLANK is low. OUTn is not turned on when BLANK is high. The timing is shown in Figure 18. All outputs are turned off at the XLAT rising edge. After that, each output is controlled again from the first clock of the internal oscillator for the next display period, based on the latest grayscale data.

When the IC is powered on, the data in the grayscale data shift register and latch are not set to default values. Therefore, grayscale data must be written to the GS latch before turning on the constant current output. BLANK should be at a high level when powered on to keep the outputs off until valid grayscale data are written to the latch. This avoids the LED being randomly illuminated immediately after power-up. If having the outputs turn on at power-up is not a problem for the application, then BLANK does not need to be held high. The grayscale functions can be controlled directly by grayscale data writing, even though BLANK is connected to GND.

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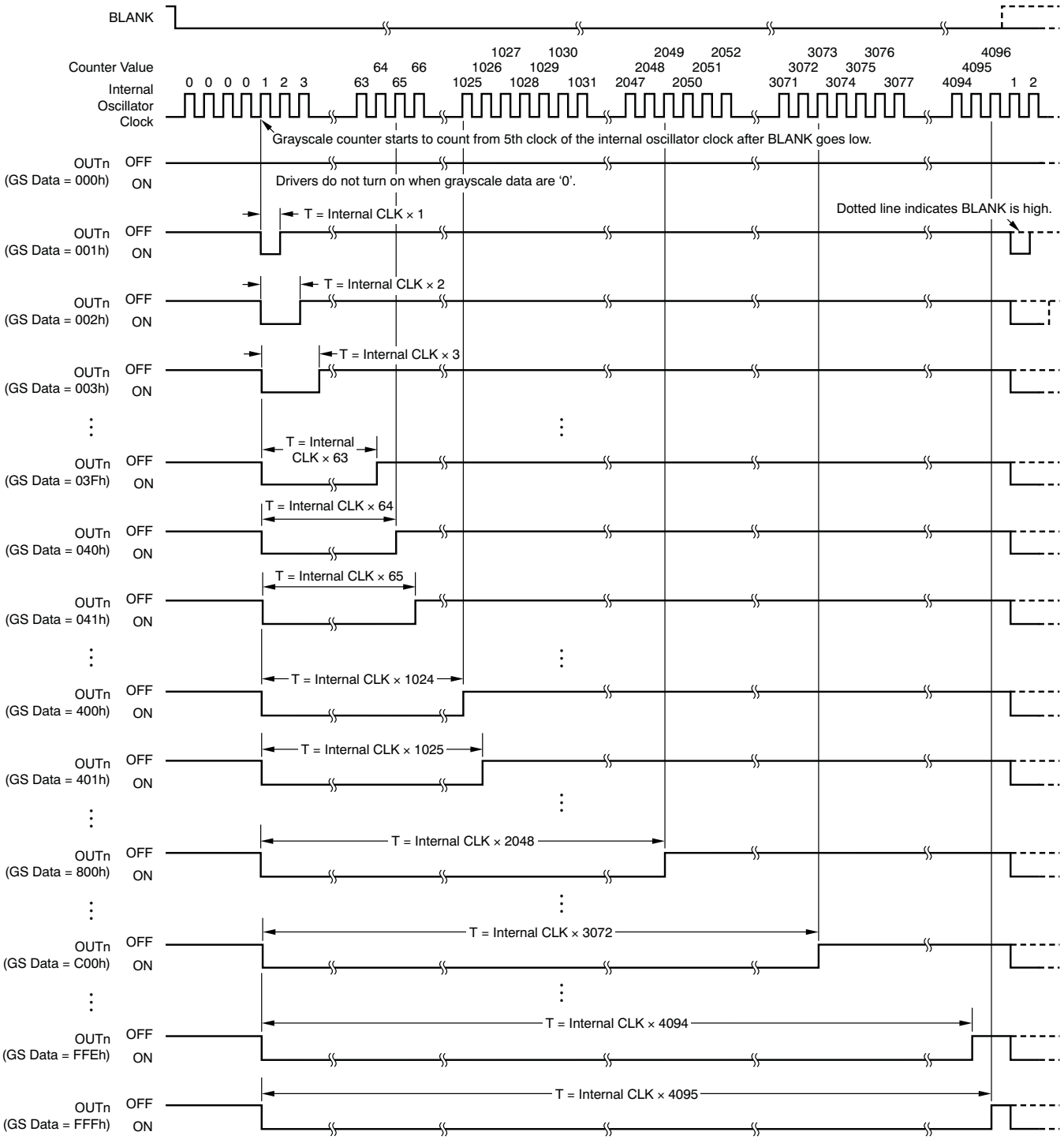

Figure 18. PWM Operation

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REGISTER CONFIGURATION

The TLC5947 has a grayscale (GS) data shift register and data latch. Both the GS data shift register and latch are 288 bits long and are used to set the PWM timing for the constant current driver. Table 2 shows the on duty cycle for each GS data. Figure 19 shows the shift register and data latch configuration. The data at the SIN pin are shifted to the LSB of the shift register at the rising edge of the SCLK pin; SOUT data are shifted out on the falling edge of SCLK. The timing diagram for data writing is shown in Figure 20. The driver on duty is controlled by the data in the GS data latch.

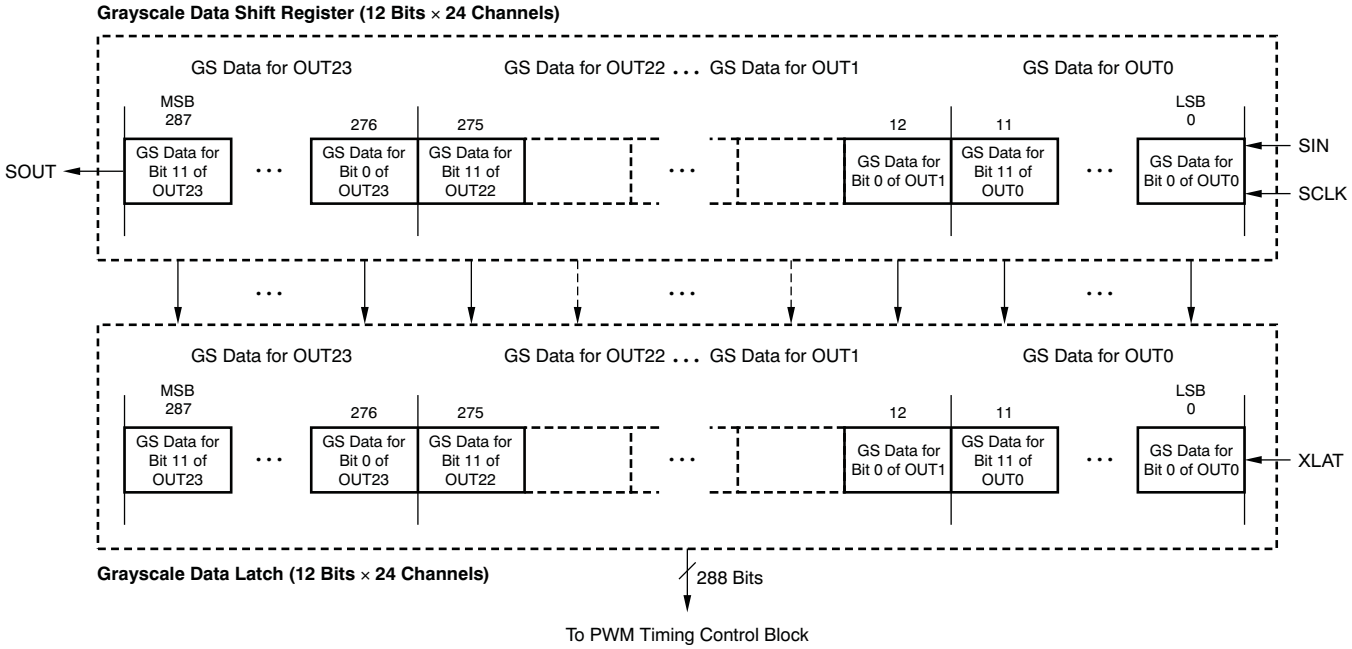

Figure 19. Grayscale Data Shift Register and Latch Configuration

Table 2. GS Data versus On Duty

GS DATA (Binary)	GS DATA (Decimal)	GS DATA (Hex)	DUTY OF DRIVER TURN-ON TIME (%)
0000 0000 0000	0	000	0.00
0000 0000 0001	1	001	0.02
0000 0000 0010	2	002	0.05
0000 0000 0011	3	003	0.07
—	—	—	—
0111 1111 1111	2047	7FF	49.98
1000 0000 0000	2048	800	50.00
1000 0000 0001	2049	801	50.02
—	—	—	—
1111 1111 1101	4093	FFD	99.93
1111 1111 1110	4094	FFE	99.95
1111 1111 1111	4095	FFF	99.98

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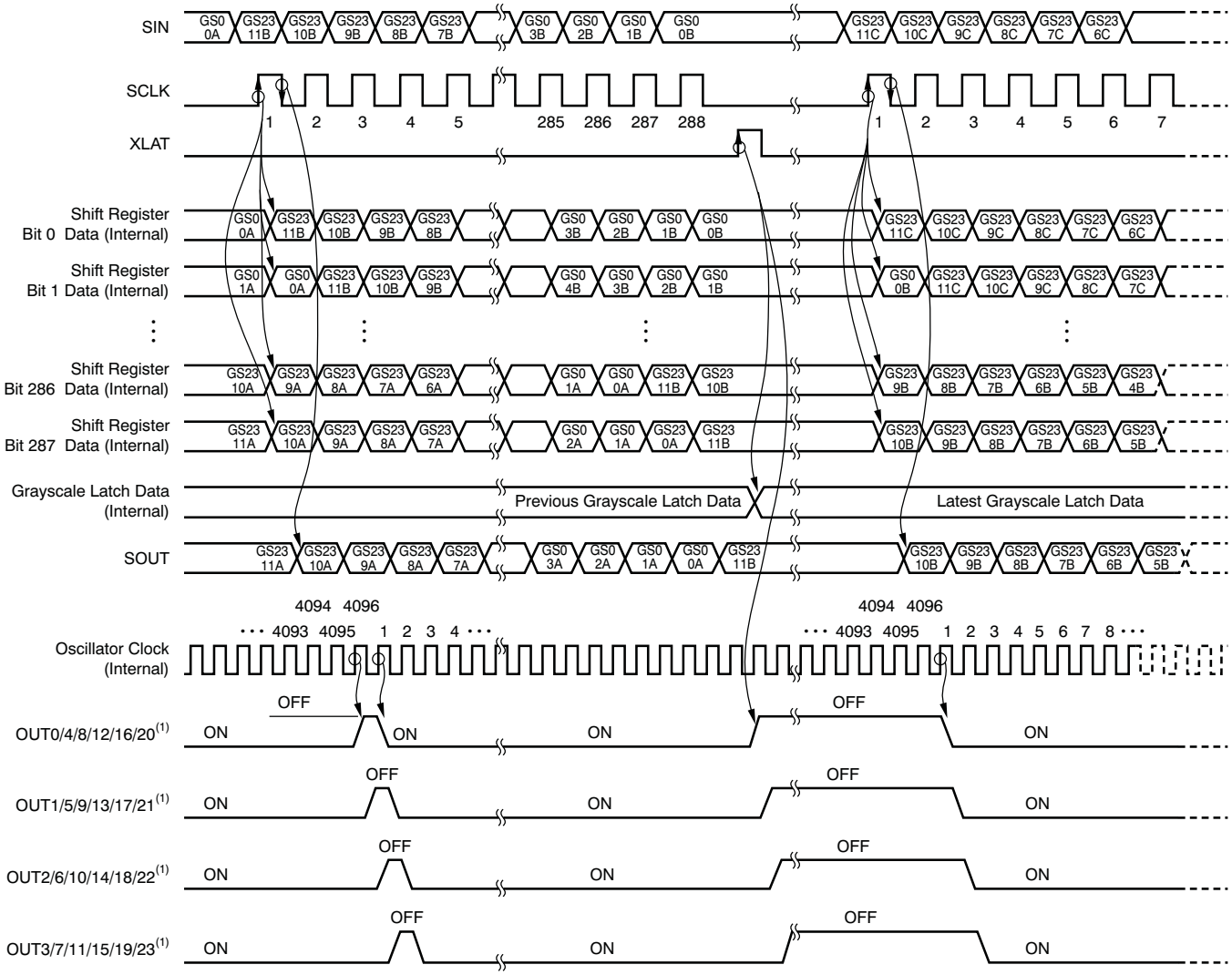
GS data are transferred from the shift register to the latch by the rising edge of XLAT. When powered up, the data in the grayscale shift register and data latch are not set to default values. Therefore, grayscale data must be written to the GS latch before turning on the constant current output. BLANK should be at a high level when powered on to avoid falsely turning on the constant current outputs due to random values in the latch at power-up. All of the constant current outputs are forced off when BLANK is high. However, if the random values turning on at power-up is not a concern in the application, BLANK can be at any level. GS can be controlled correctly with the grayscale data writing functions, even if BLANK is connected to GND. Equation 2 determines each output on duty.

$$\text{On Duty (\%)} = \frac{\text{GSn}}{4096} \times 100 \tag{2}$$

where:

GSn = the programmed grayscale value for OUTn (GSn = 0 to 4095)



(1) GS data = FFFh.

Figure 20. Grayscale Data Write Operation

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AUTO DISPLAY REPEAT FUNCTION

This function can repeat the total display period without any timing control signal, as shown in Figure 21.

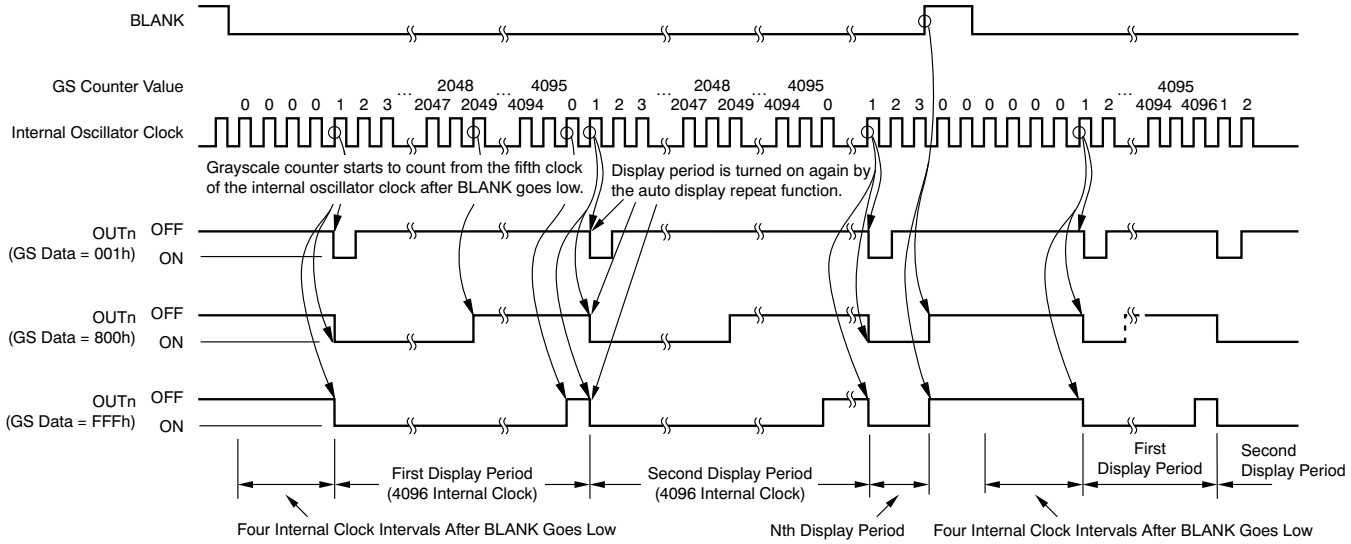

Figure 21. Auto Display Repeat Operation

THERMAL SHUTDOWN (TSD)

The thermal shutdown (TSD) function turns off all constant current outputs immediately when the IC junction temperature exceeds the high temperature threshold ($T_{(TEF)}$ = +162°C, typ). The outputs will remain disabled as long as the over-temperature condition exists. The outputs are turned on again at the first clock after the IC junction temperature falls below the temperature of $T_{(TEF)} - T_{(HYS)}$. Figure 22 shows the TSD operation.

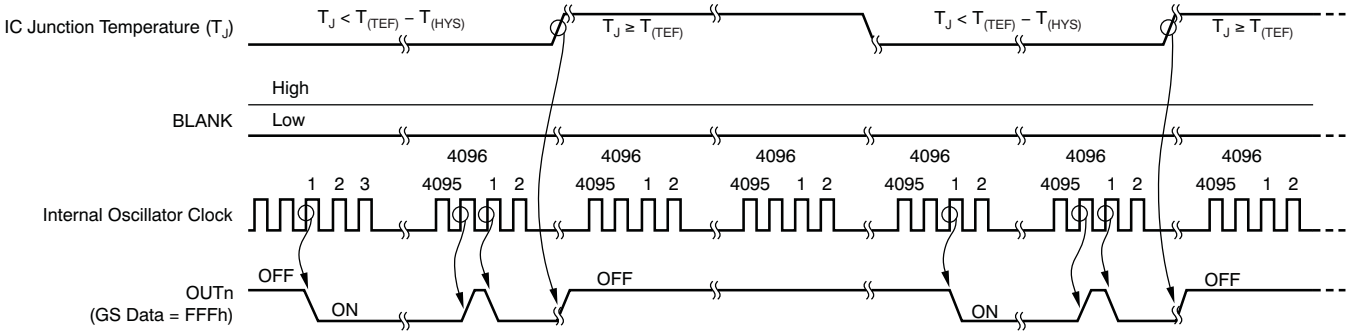

Figure 22. TSD Operation

NOISE REDUCTION

Large surge currents may flow through the IC and the board on which the device is mounted if all 24 LED channels turn on simultaneously at the start of each grayscale cycle. These large current surges could introduce detrimental noise and electromagnetic interference (EMI) into other circuits. The TLC5947 turns on the LED channels in a series delay, to provide a current soft-start feature. The output current sinks are grouped into four groups of six channels each. The first group is OUT0, 4, 8, 12, 16, 20; the second group is OUT1, 5, 9, 13, 17, 21; the third group is OUT2, 6, 10, 14, 18, 22; and the fourth group is OUT3, 7, 11, 15, 19, 23. Each group turns on sequentially with a small delay between groups; see Figure 9. Both turn-on and turn-off are delayed.

POWER DISSIPATION CALCULATION

The device power dissipation must be below the power dissipation rate of the device package (illustrated in Figure 11) to ensure correct operation. Equation 3 calculates the power dissipation of the device:

$$P_D = (V_{CC} \times I_{CC}) + (V_{OUT} \times I_{OLC} \times N \times d_{PWM}) \quad (3)$$

Where:

- V_{CC} = device supply voltage
- I_{CC} = device supply current
- V_{OUT} = OUTn voltage when driving LED current
- I_{OLC} = LED current adjusted by R_{IREF} resistor
- N = number of OUTn driving LED at the same time
- d_{PWM} = duty ratio defined by GS value

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
HPA01054DAPR	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TLC5947DAP	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TLC5947DAPG4	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TLC5947DAPR	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TLC5947DAPRG4	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TLC5947RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TLC5947RHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TLC5947RHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TLC5947RHBTG4	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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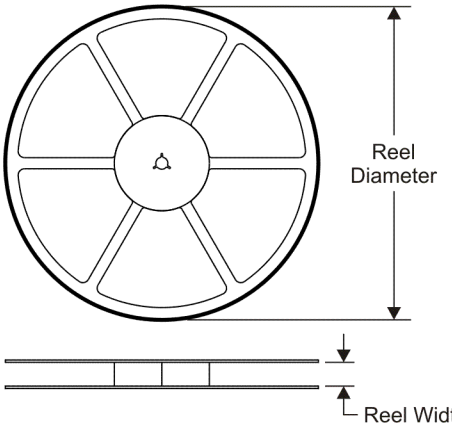
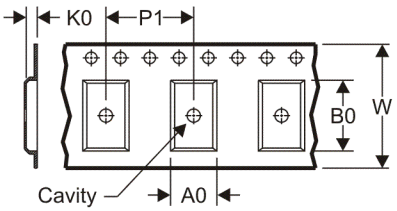
TAPE AND REEL INFORMATION

REEL DIMENSIONS

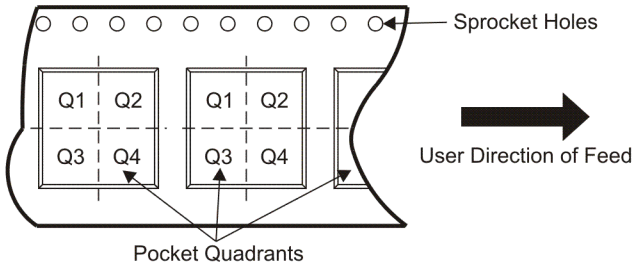


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

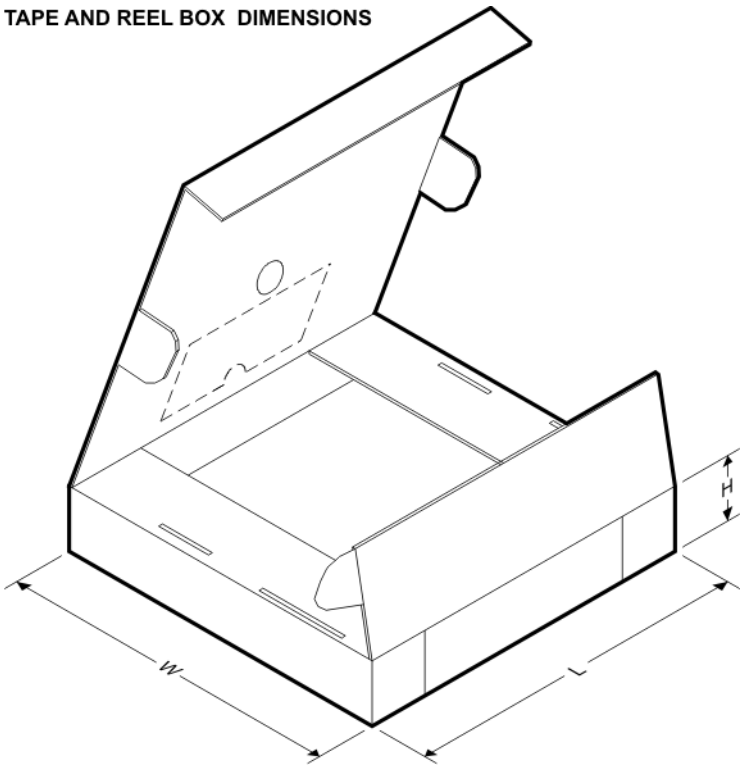
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5947DAPR	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1
TLC5947RHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TLC5947RHBT	QFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

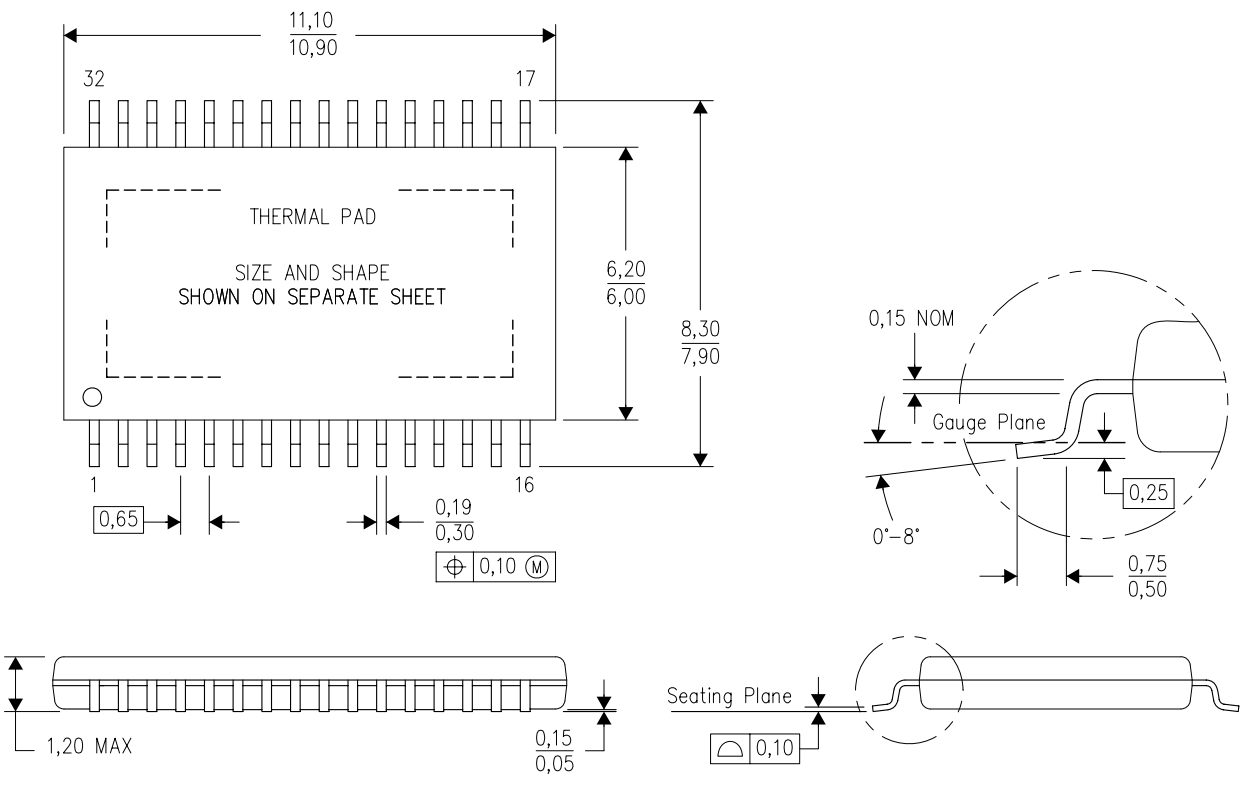
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5947DAPR	HTSSOP	DAP	32	2000	346.0	346.0	41.0
TLC5947RHBR	QFN	RHB	32	3000	346.0	346.0	29.0
TLC5947RHBT	QFN	RHB	32	250	190.5	212.7	31.8

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
F. Falls within JEDEC MO–153 Variation DCT.

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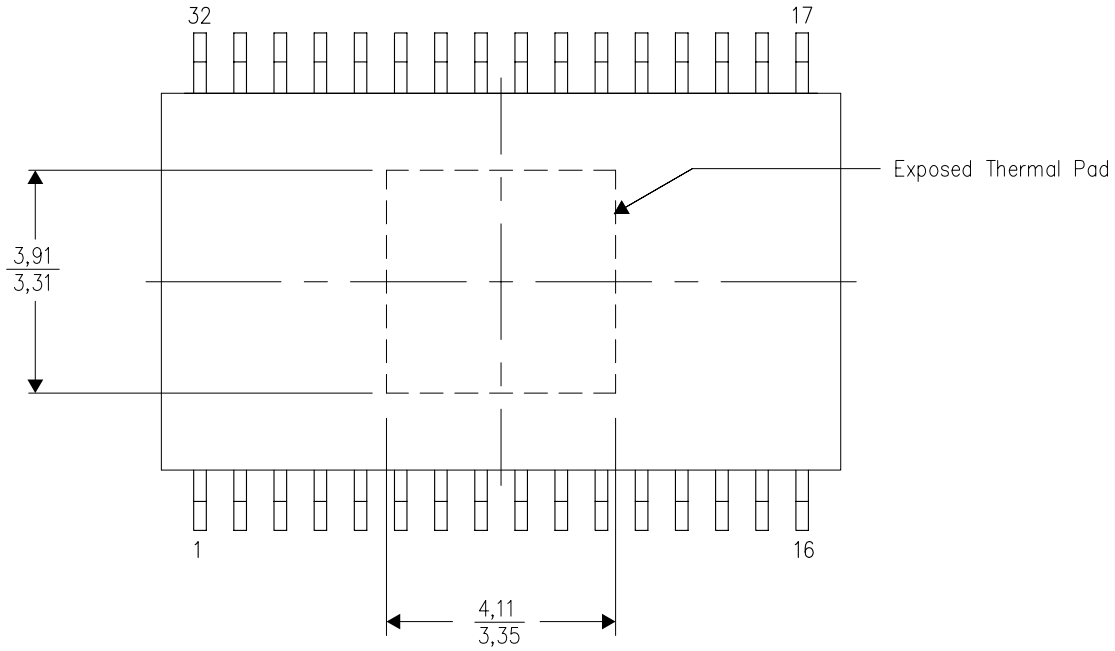
DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

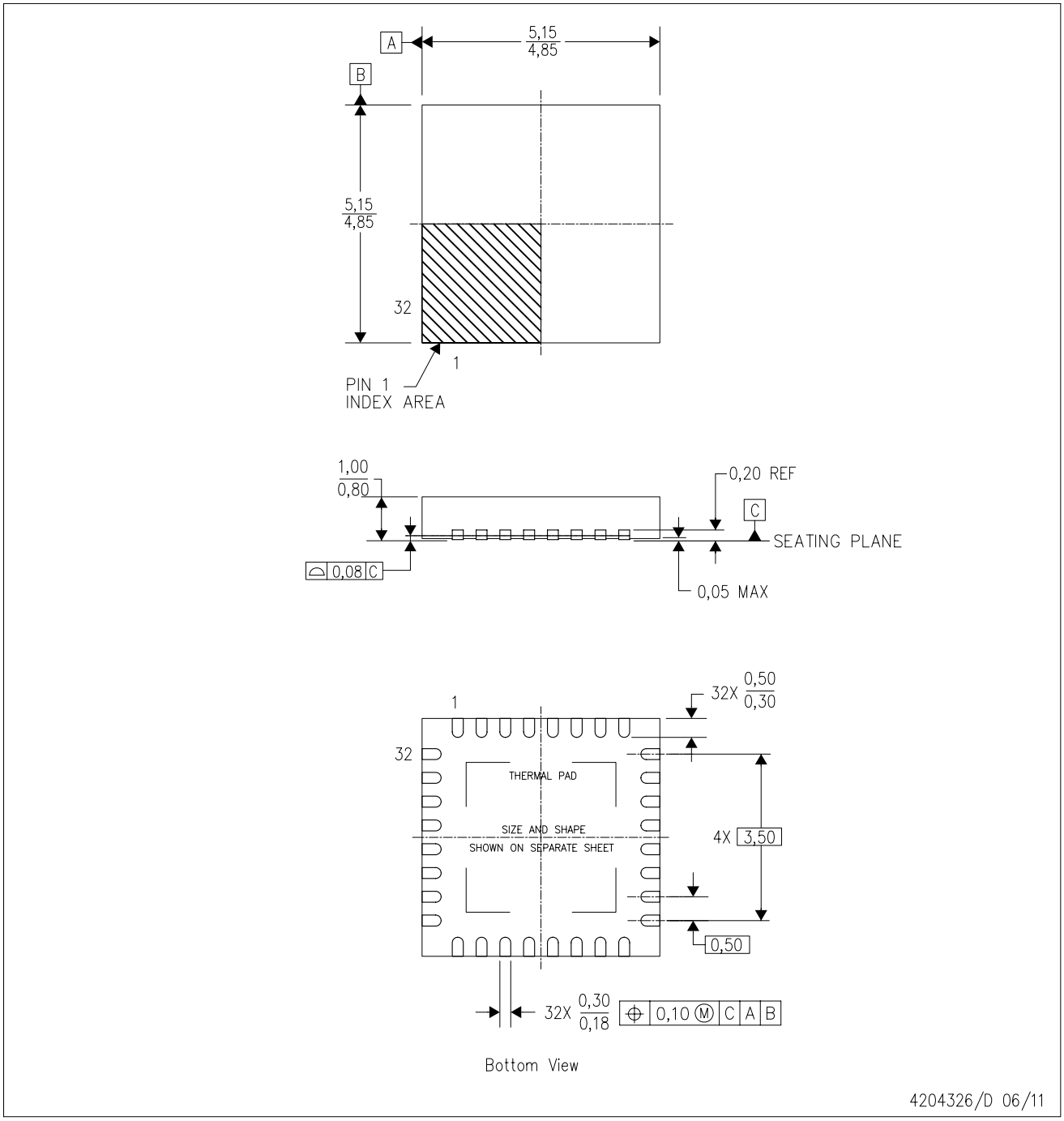
Exposed Thermal Pad Dimensions

4206319–3/I 07/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Insrtuments.

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

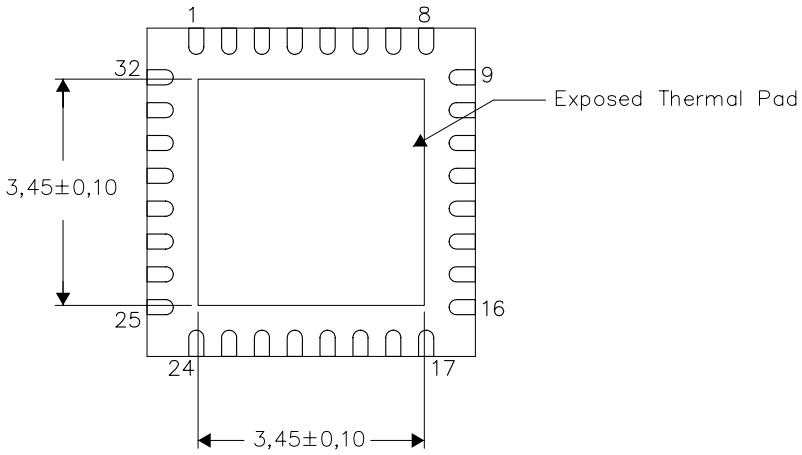
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



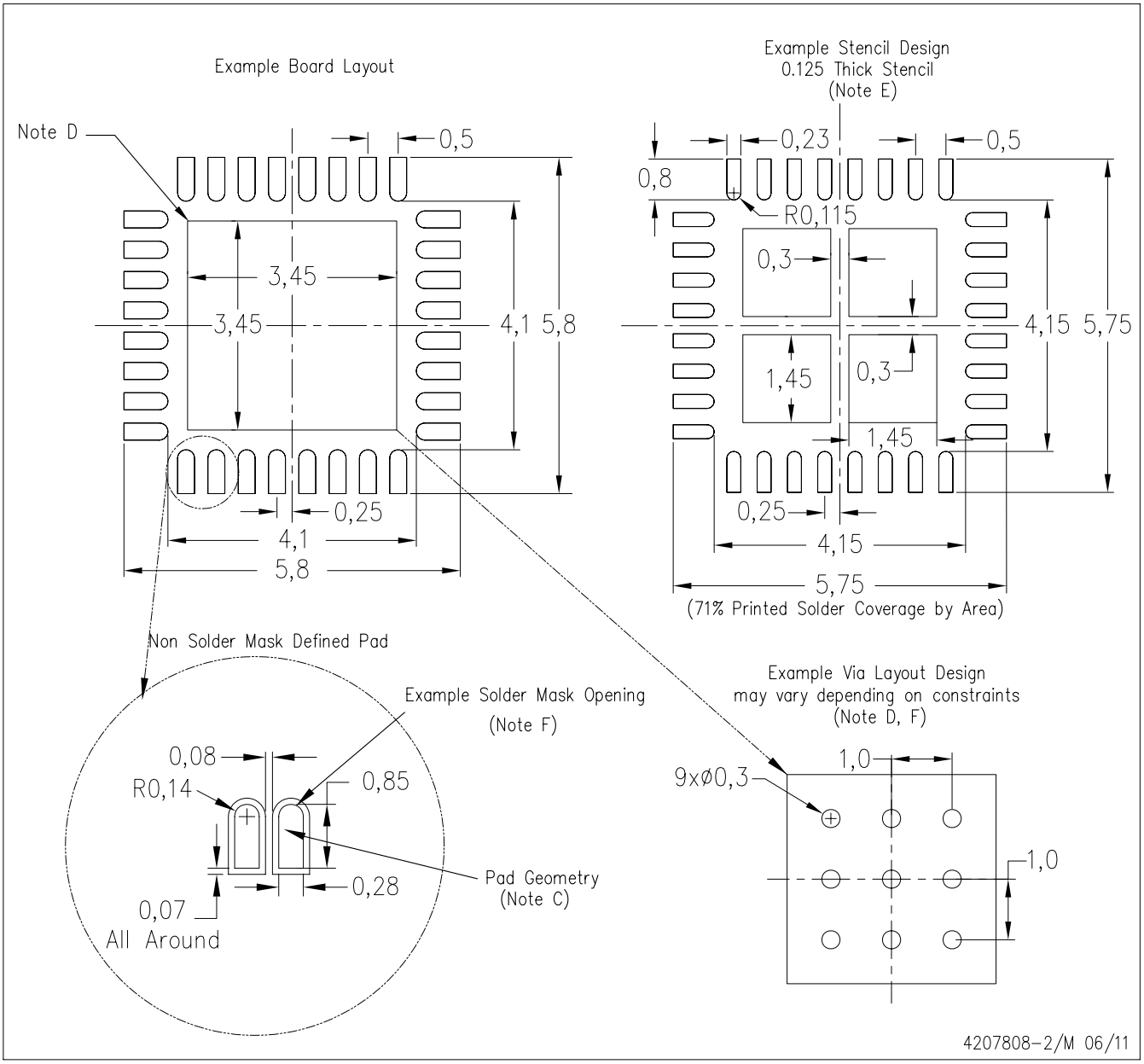
Bottom View

Exposed Thermal Pad Dimensions

4206356–2/U 06/11

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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RFID	www.ti-rfid.com		
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