



HESTORE.HU

elektronikai alkatrész áruház

EN: This Datasheet is presented by the manufacturer.

Please visit our website for pricing and availability at www.hestore.hu.

CD4051BC • CD4052BC • CD4053BC

Single 8-Channel Analog Multiplexer/Demultiplexer • Dual 4-Channel Analog Multiplexer/Demultiplexer • Triple 2-Channel Analog Multiplexer/Demultiplexer

General Description

The CD4051BC, CD4052BC, and CD4053BC analog multiplexers/demultiplexers are digitally controlled analog switches having low "ON" impedance and very low "OFF" leakage currents. Control of analog signals up to $15V_{p-p}$ can be achieved by digital signal amplitudes of 3–15V. For example, if $V_{DD} = 5V$, $V_{SS} = 0V$ and $V_{EE} = -5V$, analog signals from $-5V$ to $+5V$ can be controlled by digital inputs of 0–5V. The multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD}-V_{SS}$ and $V_{DD}-V_{EE}$ supply voltage ranges, independent of the logic state of the control signals. When a logical "1" is present at the inhibit input terminal all channels are "OFF".

CD4051BC is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned "ON" and connect the input to the output.

CD4052BC is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 or 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

CD4053BC is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

Features

- Wide range of digital and analog signal levels: digital 3 – 15V, analog to $15V_{p-p}$
- Low "ON" resistance: 80Ω (typ.) over entire $15V_{p-p}$ signal-input range for $V_{DD} - V_{EE} = 15V$
- High "OFF" resistance: channel leakage of ± 10 pA (typ.) at $V_{DD} - V_{EE} = 10V$
- Logic level conversion for digital addressing signals of 3 – 15V ($V_{DD} - V_{SS} = 3 - 15V$) to switch analog signals to $15V_{p-p}$ ($V_{DD} - V_{EE} = 15V$)
- Matched switch characteristics: $\Delta R_{ON} = 5\Omega$ (typ.) for $V_{DD} - V_{EE} = 15V$
- Very low quiescent power dissipation under all digital-control input and supply conditions: $1 \mu W$ (typ.) at $V_{DD} - V_{SS} = V_{DD} - V_{EE} = 10V$
- Binary address decoding on chip

Ordering Code:

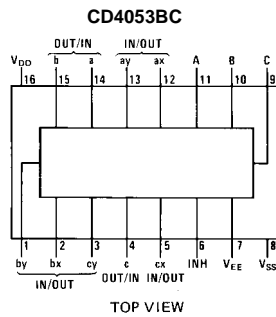
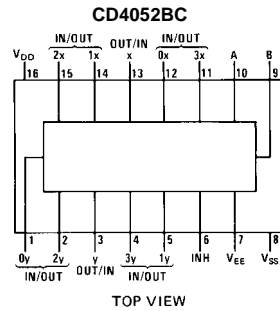
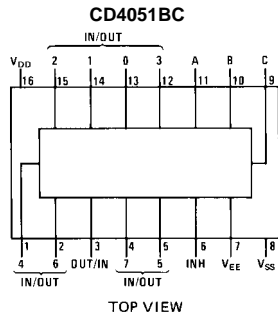
| Order Number | Package Number | Package Description |
|--------------|----------------|--|
| CD4051BCM | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| CD4051BCSJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| CD4051BCMTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| CD4051BCN | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| CD4052BCM | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| CD4052BCSJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| CD4052BCN | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| CD4053BCM | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| CD4053BCSJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| CD4053BCN | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

CD4051BC • CD4052BC • CD4053BC Single 8-Channel Analog Multiplexer/Demultiplexer • Dual 4-Channel Analog Multiplexer/Demultiplexer • Triple 2-Channel Analog Multiplexer/Demultiplexer

Connection Diagrams

Pin Assignments for DIP and SOIC



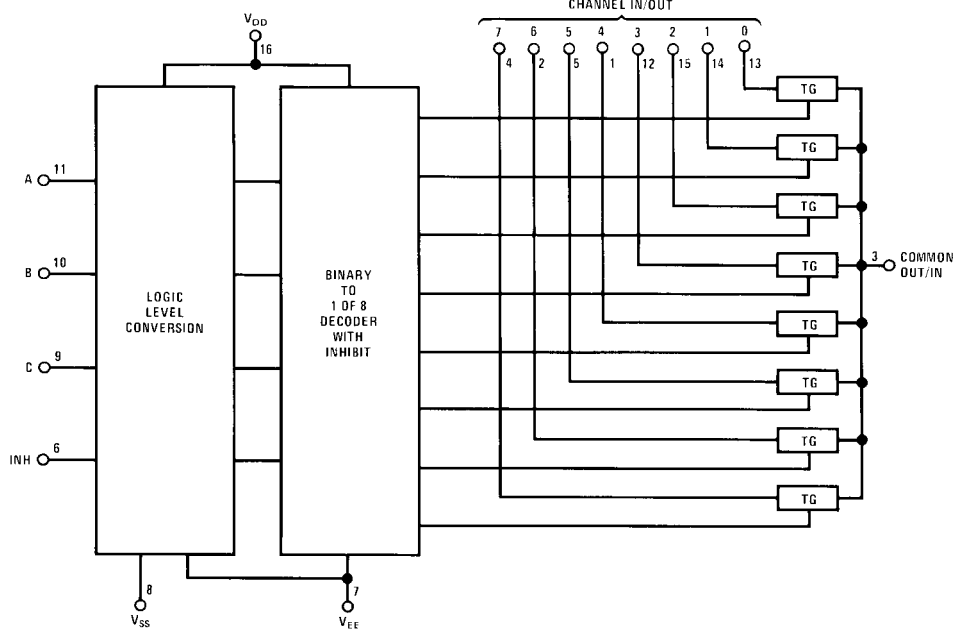
Truth Table

| INPUT STATES | | | | "ON" CHANNELS | | |
|--------------|---|---|---|---------------|---------|------------|
| INHIBIT | C | B | A | CD4051B | CD4052B | CD4053B |
| 0 | 0 | 0 | 0 | 0 | 0X, 0Y | cx, bx, ax |
| 0 | 0 | 0 | 1 | 1 | 1X, 1Y | cx, bx, ay |
| 0 | 0 | 1 | 0 | 2 | 2X, 2Y | cx, by, ax |
| 0 | 0 | 1 | 1 | 3 | 3X, 3Y | cx, by, ay |
| 0 | 1 | 0 | 0 | 4 | | cy, bx, ax |
| 0 | 1 | 0 | 1 | 5 | | cy, bx, ay |
| 0 | 1 | 1 | 0 | 6 | | cy, by, ax |
| 0 | 1 | 1 | 1 | 7 | | cy, by, ay |
| 1 | * | * | * | NONE | NONE | NONE |

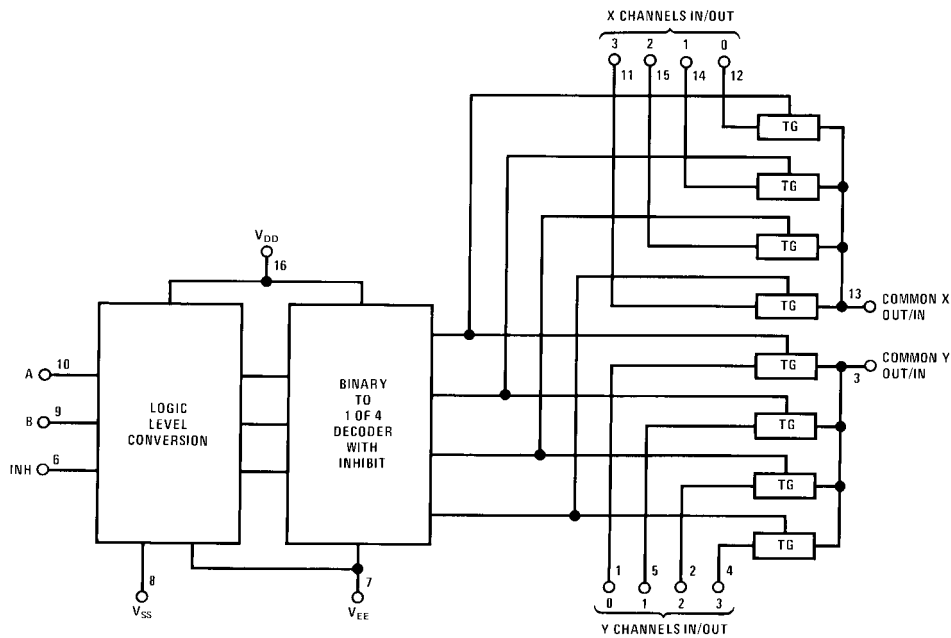
*Don't Care condition.

Logic Diagrams

CD4051BC

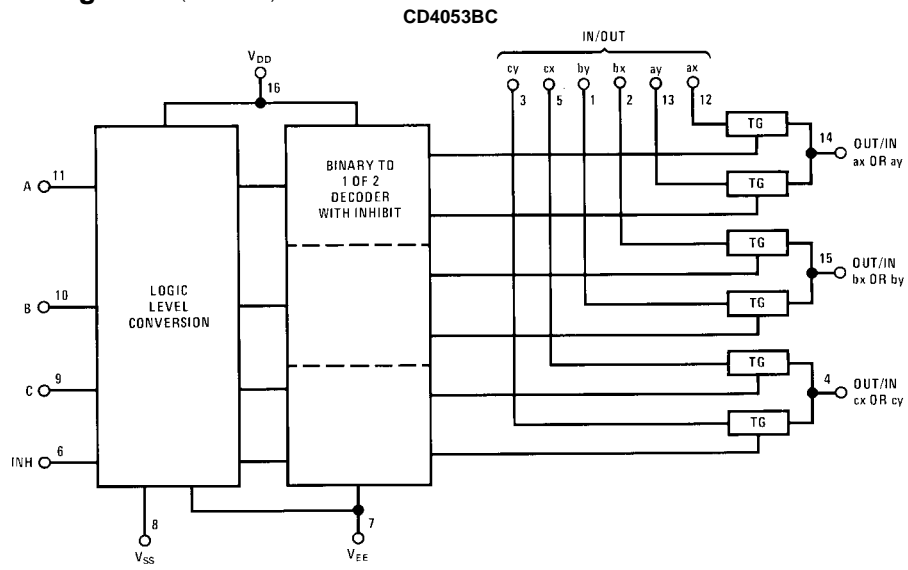


CD4052BC



CD4051BC • CD4052BC • CD4053BC

Logic Diagrams (Continued)



| Absolute Maximum Ratings (Note 1) | | Recommended Operating Conditions | |
|--|---|---------------------------------------|--|
| DC Supply Voltage (V_{DD}) | -0.5 V_{DC} to +18 V_{DC} | DC Supply Voltage (V_{DD}) | +5 V_{DC} to +15 V_{DC} |
| Input Voltage (V_{IN}) | -0.5 V_{DC} to V_{DD} +0.5 V_{DC} | Input Voltage (V_{IN}) | 0V to V_{DD} V_{DC} |
| Storage Temperature Range (T_S) | -65°C to +150°C | Operating Temperature Range (T_A) | CD4051BC/CD4052BC/CD4053BC -55°C to +125°C |
| Power Dissipation (P_D) | | | |
| Dual-In-Line | 700 mW | | |
| Small Outline | 500 mW | | |
| Lead Temperature (T_L) (soldering, 10 seconds) | 260°C | | |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics tables provide conditions for actual device operation.

DC Electrical Characteristics (Note 2)

| Symbol | Parameter | Conditions | -55°C | | +25° | | | 125°C | | Units | |
|--|--|---|--|---------------|------|-------------------|---------------|-------|-------------------|---------|----------|
| | | | Min | Max | Min | Typ | Max | Min | Max | | |
| Control A, B, C and Inhibit | | | | | | | | | | | |
| I_{IN} | Input Current | $V_{DD} = 15V, V_{EE} = 0V$ $V_{IN} = 0V$ | | -0.1 | | -10 ⁻⁵ | -0.1 | | -1.0 | μA | |
| | | $V_{DD} = 15V, V_{EE} = 0V$ $V_{IN} = 15V$ | | 0.1 | | 10 ⁻⁵ | 0.1 | | 1.0 | | |
| I_{DD} | Quiescent Device Current | $V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$ | | 5 10 20 | | | 5 10 20 | | 150 300 600 | μA | |
| Signal Inputs (V_{IS}) and Outputs (V_{OS}) | | | | | | | | | | | |
| R_{ON} | "ON" Resistance (Peak for $V_{EE} \leq V_{IS} \leq V_{DD}$) | $R_L = 10\text{ k}\Omega$ (any channel selected) | $V_{DD} = 2.5V, V_{EE} = -2.5V$ or $V_{DD} = 5V, V_{EE} = 0V$ | | 800 | | 270 | 1050 | | 1300 | Ω |
| | | | $V_{DD} = 5V, V_{EE} = -5V$ or $V_{DD} = 10V, V_{EE} = 0V$ | | 310 | | 120 | 400 | | 550 | Ω |
| | | | $V_{DD} = 7.5V, V_{EE} = -7.5V$ or $V_{DD} = 15V, V_{EE} = 0V$ | | 200 | | 80 | 240 | | 320 | Ω |
| ΔR_{ON} | Δ "ON" Resistance Between Any Two Channels | $R_L = 10\text{ k}\Omega$ (any channel selected) | $V_{DD} = 2.5V, V_{EE} = -2.5V$ or $V_{DD} = 5V, V_{EE} = 0V$ | | | | 10 | | | | Ω |
| | | | $V_{DD} = 5V, V_{EE} = -5V$ or $V_{DD} = 10V, V_{EE} = 0V$ | | | | 10 | | | | Ω |
| | | | $V_{DD} = 7.5V, V_{EE} = -7.5V$ or $V_{DD} = 15V, V_{EE} = 0V$ | | | | 5 | | | | Ω |
| | "OFF" Channel Leakage Current, any channel "OFF" | $V_{DD} = 7.5V, V_{EE} = -7.5V$ $O/I = \pm 7.5V, I/O = 0V$ | | ± 50 | | ± 0.01 | ± 50 | | ± 500 | nA | |
| | "OFF" Channel Leakage Current, all channels | Inhibit = 7.5V $V_{DD} = 7.5V, V_{EE} = -7.5V, O/I = 0V$ | | ± 200 | | ± 0.08 | ± 200 | | ± 2000 | nA | |
| | "OFF" (Common OUT/IN) | $V_{DD} = 7.5V, V_{EE} = -7.5V, O/I = 0V$ $I/O = \pm 7.5V$ | | ± 200 | | ± 0.04 | ± 200 | | ± 2000 | nA | |
| | | | | ± 200 | | ± 0.02 | ± 200 | | ± 2000 | nA | |

| DC Electrical Characteristics (Continued) | | | | | | | | | | |
|---|--------------------------|--|-------|-----|------|-----|-----|-------|-----|-------|
| Symbol | Parameter | Conditions | -55°C | | +25° | | | 125°C | | Units |
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| Control Inputs A, B, C and Inhibit | | | | | | | | | | |
| V_{IL} | LOW Level Input Voltage | $V_{EE} = V_{SS}$ $R_L = 1\text{ k}\Omega$ to V_{SS} $I_{IS} < 2\text{ }\mu\text{A}$ on all OFF Channels $V_{IS} = V_{DD}$ thru $1\text{ k}\Omega$ $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$ | | | | | | | | |
| | | | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 3.0 | | | 3.0 | | 3.0 | V |
| | | | | 4.0 | | | 4.0 | | 4.0 | V |
| V_{IH} | HIGH Level Input Voltage | $V_{DD} = 5$ $V_{DD} = 10$ $V_{DD} = 15$ | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | 7 | | 7 | | | 7 | | V |
| | | | 11 | | 11 | | | 11 | | V |
| <p>Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.</p> | | | | | | | | | | |

| AC Electrical Characteristics (Note 3) | | | | | | | |
|--|---|---|-------------------|-----|-------------------|--------------------|-----------|
| $T_A = 25^\circ\text{C}$, $t_r = t_f = 20\text{ ns}$, unless otherwise specified. | | | | | | | |
| Symbol | Parameter | Conditions | V_{DD} | Min | Typ | Max | Units |
| t_{PZH} , t_{PZL} | Propagation Delay Time from Inhibit to Signal Output (channel turning on) | $V_{EE} = V_{SS} = 0V$ $R_L = 1\text{ k}\Omega$ $C_L = 50\text{ pF}$ | 5V 10V 15V | | 600 225 160 | 1200 450 320 | ns |
| t_{PHZ} , t_{PLZ} | Propagation Delay Time from Inhibit to Signal Output (channel turning off) | $V_{EE} = V_{SS} = 0V$ $R_L = 1\text{ k}\Omega$ $C_L = 50\text{ pF}$ | 5V 10V 15V | | 210 100 75 | 420 200 150 | ns |
| C_{IN} | Input Capacitance Control input Signal Input (IN/OUT) | | | | 5 10 | 7.5 15 | pF |
| C_{OUT} | Output Capacitance (common OUT/IN) | | | | | | |
| | CD4051 CD4052 CD4053 | $V_{EE} = V_{SS} = 0V$ | 10V 10V 10V | | 30 15 8 | | pF |
| C_{IOS} | Feedthrough Capacitance | | | | 0.2 | | pF |
| C_{PD} | Power Dissipation Capacitance | | | | | | |
| | CD4051 CD4052 CD4053 | | | | 110 140 70 | | pF |
| Signal Inputs (V_{IS}) and Outputs (V_{OS}) | | | | | | | |
| | Sine Wave Response (Distortion) | $R_L = 10\text{ k}\Omega$ $f_{IS} = 1\text{ kHz}$ $V_{IS} = 5\text{ V}_{p-p}$ $V_{EE} = V_{SI} = 0V$ | 10V | | 0.04 | | % |
| | Frequency Response, Channel "ON" (Sine Wave Input) | $R_L = 1\text{ k}\Omega$, $V_{EE} = 0V$, $V_{IS} = 5V_{p-p}$, $20 \log_{10} V_{OS}/V_{IS} = -3\text{ dB}$ | 10V | | 40 | | MHz |
| | Feedthrough, Channel "OFF" | $R_L = 1\text{ k}\Omega$, $V_{EE} = V_{SS} = 0V$, $V_{IS} = 5V_{p-p}$, $20 \log_{10} V_{OS}/V_{IS} = -40\text{ dB}$ | 10V | | 10 | | MHz |
| | Crosstalk Between Any Two Channels (frequency at 40 dB) | $R_L = 1\text{ k}\Omega$, $V_{EE} = V_{SS} = 0V$, $V_{IS}(A) = 5V_{p-p}$, $20 \log_{10} V_{OS}(B)/V_{IS}(A) = -40\text{ dB}$ (Note 4) | 10V | | 3 | | MHz |
| t_{PHL} , t_{PLH} | Propagation Delay Signal Input to Signal Output | $V_{EE} = V_{SS} = 0V$ $C_L = 50\text{ pF}$ | 5V 10V 15V | | 25 15 10 | 55 35 25 | ns |
| Control Inputs, A, B, C and Inhibit | | | | | | | |
| | Control Input to Signal Crosstalk | $V_{EE} = V_{SS} = 0V$, $R_L = 10\text{ k}\Omega$ at both ends of channel. Input Square Wave Amplitude = 10V | 10V | | 65 | | mV (peak) |
| t_{PHL} , t_{PLH} | Propagation Delay Time from Address to Signal Output (channels "ON" or "OFF") | $V_{EE} = V_{SS} = 0V$ $C_L = 50\text{ pF}$ | 5V 10V 15V | | 500 180 120 | 1000 360 240 | ns |
| <p>Note 3: AC Parameters are guaranteed by DC correlated testing.</p> <p>Note 4: A, B are two arbitrary channels with A turned "ON" and B "OFF".</p> | | | | | | | |

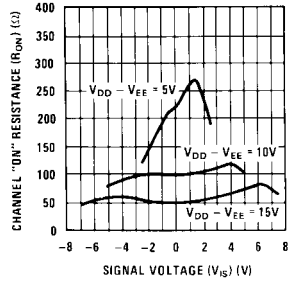
Special Considerations

In certain applications the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into IN/OUT pin, the voltage drop across the bidirectional

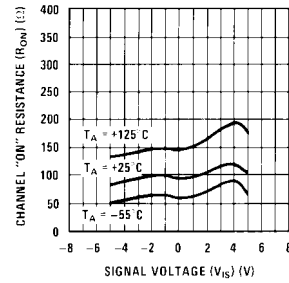
switch must not exceed 0.6V at $T_A \leq 25^\circ\text{C}$, or 0.4V at $T_A > 25^\circ\text{C}$ (calculated from R_{ON} values shown). No V_{DD} current will flow through R_L if the switch current flows into OUT/IN pin.

Typical Performance Characteristics

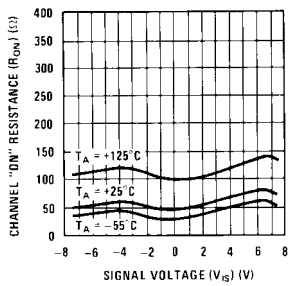
“ON” Resistance vs Signal Voltage for $T_A = 25^\circ\text{C}$



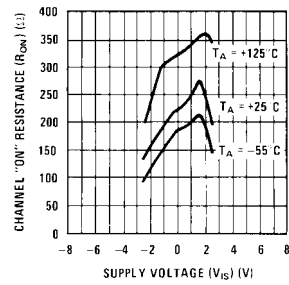
“ON” Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 10V$



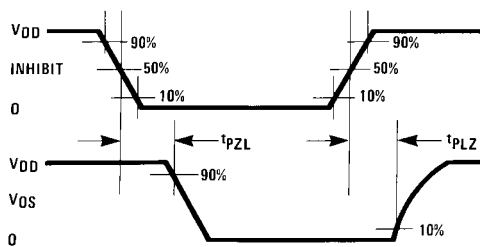
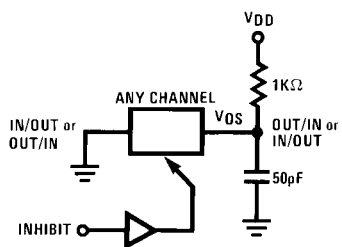
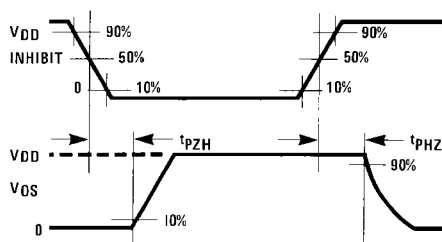
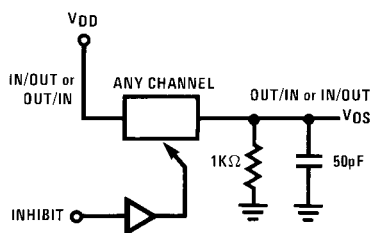
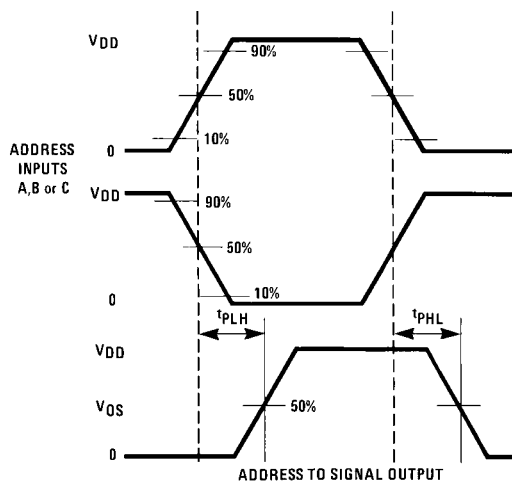
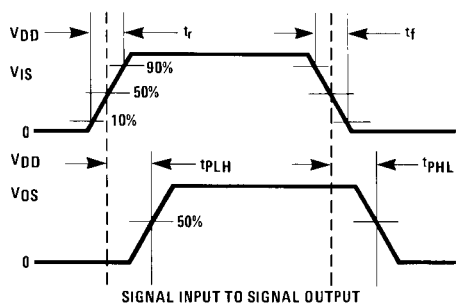
“ON” Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 15V$



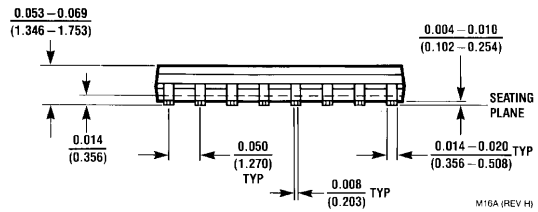
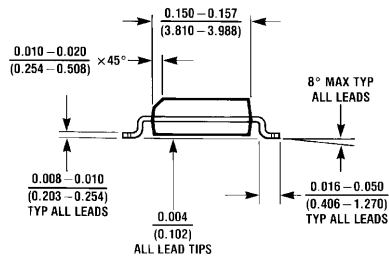
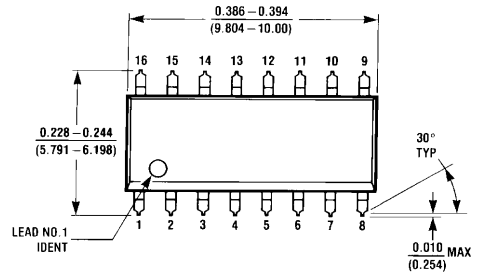
“ON” Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 5V$



Switching Time Waveforms



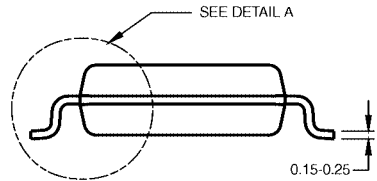
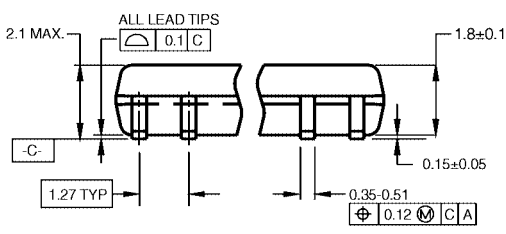
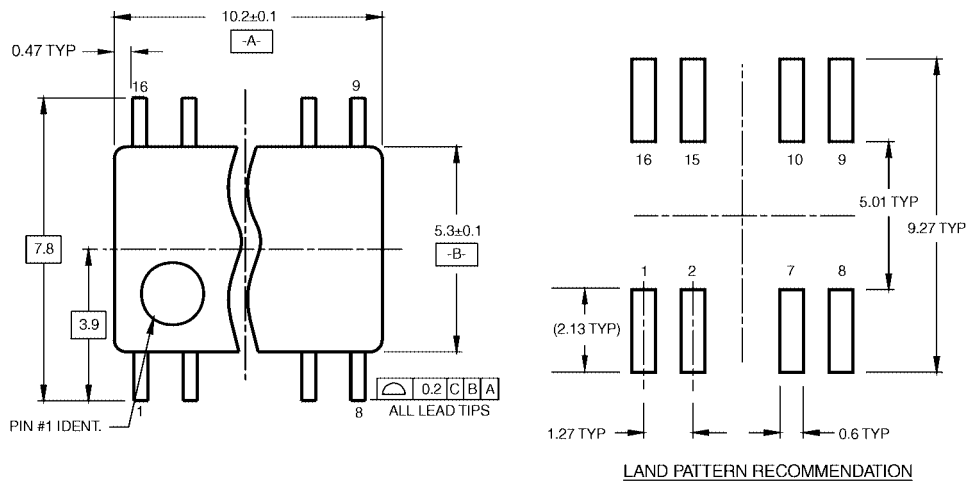
Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

M16A (REV H)

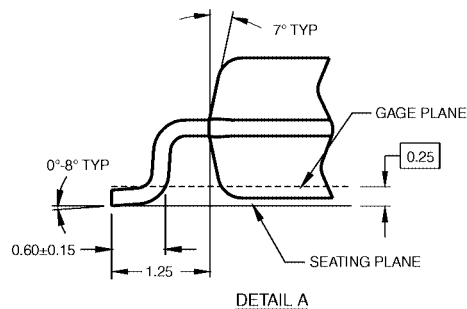
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

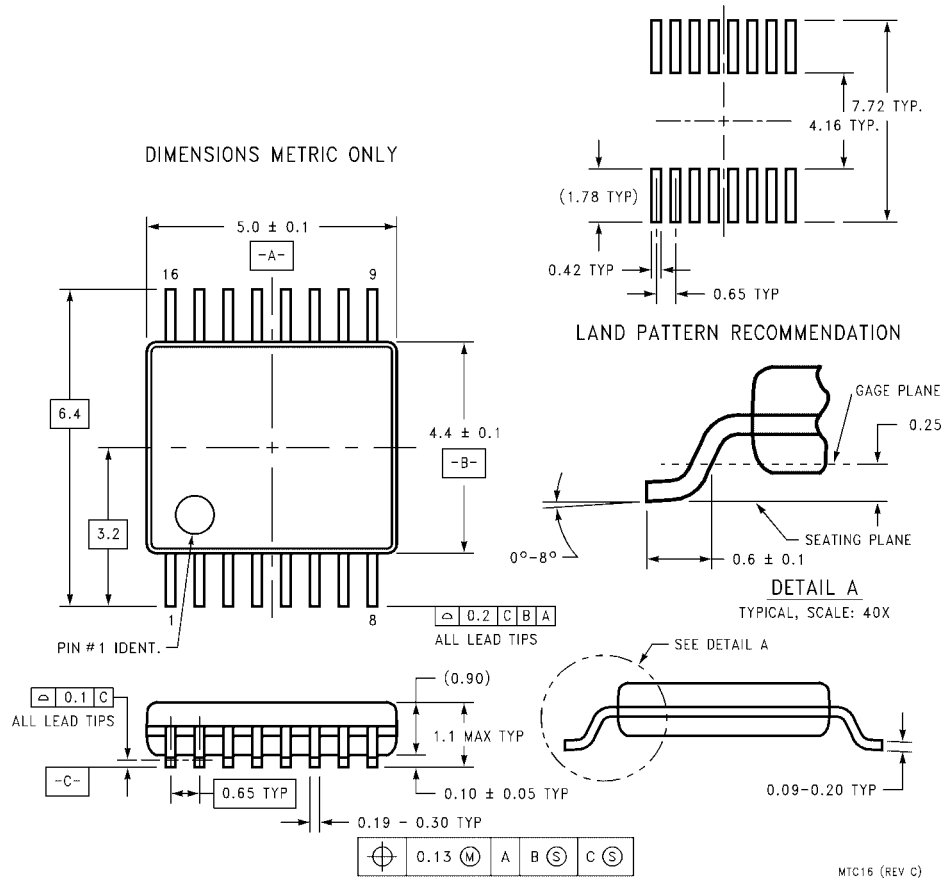
- NOTES:
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1



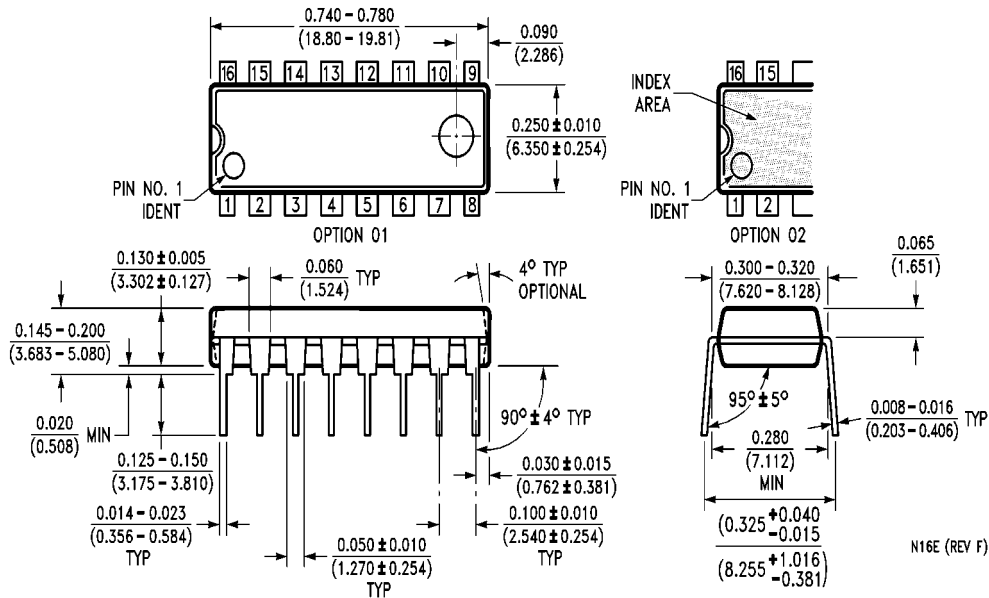
**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
 Package Number M16D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com