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# LM2940/LM2940C

## 1A Low Dropout Regulator

### General Description

The LM2940/LM2940C positive voltage regulator features the ability to source 1A of output current with a dropout voltage of typically 0.5V and a maximum of 1V over the entire temperature range. Furthermore, a quiescent current reduction circuit has been included which reduces the ground current when the differential between the input voltage and the output voltage exceeds approximately 3V. The quiescent current with 1A of output current and an input-output differential of 5V is therefore only 30 mA. Higher quiescent currents only exist when the regulator is in the dropout mode ( $V_{IN} - V_{OUT} < 3V$ ).

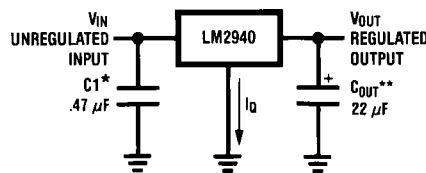
Designed also for vehicular applications, the LM2940/LM2940C and all regulated circuitry are protected from reverse battery installations or 2-battery jumps. During line transients, such as load dump when the input voltage can momentarily exceed the specified maximum operating volt-

age, the regulator will automatically shut down to protect both the internal circuits and the load. The LM2940/LM2940C cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

### Features

- Dropout voltage typically 0.5V @  $I_O = 1A$
- Output current in excess of 1A
- Output voltage trimmed before assembly
- Reverse battery protection
- Internal short circuit current limit
- Mirror image insertion protection
- P+ Product Enhancement tested

### Typical Application



882203

\*Required if regulator is located far from power supply filter.

\*\* $C_{OUT}$  must be at least 22  $\mu F$  to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator and the ESR is critical; see curve.

### Ordering Information

Temp Range	Output Voltage						Package
	5.0	8.0	9.0	10	12	15	
0 C 7T <sub>J</sub> 7 125 C	LM2940CT-5.0	∣	LM2940CT-9.0	∣	LM2940CT-12	LM2940CT-15	TO-220
	LM2940CS-5.0	∣	LM2940CS-9.0	∣	LM2940CS-12	LM2940CS-15	TO-263
	LM2940CSX-5.0	∣	LM2940CSX-9.0	∣	LM2940CSX-12	LM2940CSX-15	
40 C 7T <sub>J</sub> 7 125 C	LM2940LD-5.0	LM2940LD-8.0	LM2940LD-9.0	LM2940LD-10	LM2940LD-12	LM2940LD-15	LLP 1k Units Tape and Reel
	LM2940LDX-5.0	LM2940LDX-8.0	LM2940LDX-9.0	LM2940LDX-10	LM2940LDX-12	LM2940LDX-15	LLP 4.5k Units Tape and Reel
40 C 7T <sub>J</sub> 7 125 C	LM2940T-5.0	LM2940T-8.0	LM2940T-9.0	LM2940T-10	LM2940T-12	∣	TO-220
	LM2940S-5.0	LM2940S-8.0	LM2940S-9.0	LM2940S-10	LM2940S-12	∣	TO-263
	LM2940SX-5.0	LM2940SX-8.0	LM2940SX-9.0	LM2940SX-10	LM2940SX-12	∣	

Temp Range	Output Voltage						Package
	5.0	8.0	9.0	10	12	15	
40 C	LM2940IMP-5.0	LM2940IMP-8.0	LM2940IMP-9.0	LM2940IMP-10	LM2940IMP-12	LM2940IMP-15	SOT-223
7T <sub>A</sub> 7 85 C	LM2940IMPX -5.0	LM2940IMPX -8.0	LM2940IMPX -9.0	LM2940IMPX -10	LM2940IMPX -12	LM2940IMPX -15	SOT-223 in Tape and Reel
Marking	L53B	L54B	L0EB	L55B	L56B	L70B	

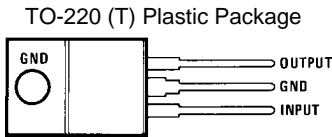
The physical size of the SOT-223 is too small to contain the full device part number. The package markings indicated are what will appear on the actual device.

Mil-Aero Ordering Information

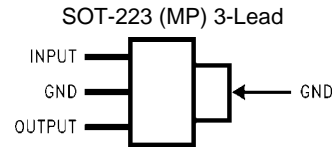
Temperature Range	Output Voltage				Package
	5.0	8.0	12	15	
55 C	LM2940J-5.0/883 5962-8958701EA	;	LM2940J-12/883 5962-9088401QEA	LM2940J-15/883 5962-9088501QEA	J16A
7T <sub>J</sub> 7 125 C	LM2940WG5.0/883 5962-8958701XA	;	LM2940WG5-12/883	LM2940WG5-15/883	WG16A

For information on military temperature range products, please go to the Mil/Aero Web Site at <http://www.national.com/appinfo/milaero/index.html>.

Connection Diagrams

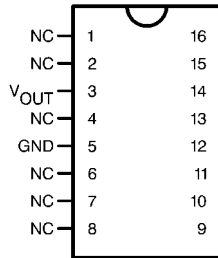


882202  
Front View  
See NS Package Number TO3B



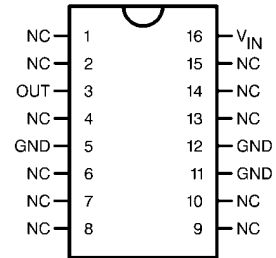
882242  
Front View  
See NS Package Number MP04A

16-Lead Dual-in-Line Package (J)



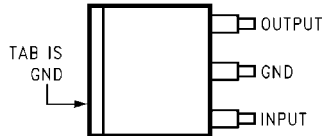
882243  
Top View  
See NS Package Number J16A

16-Lead Ceramic Surface-Mount Package (WG)



882244  
Top View  
See NS Package Number WG16A

TO-263 (S) Surface-Mount Package

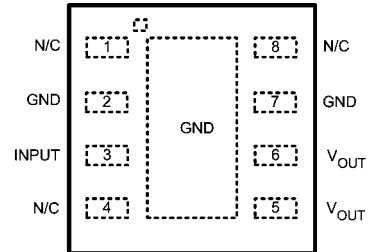


882211  
Top View



882212  
Side View  
See NS Package Number TS3B

LLP (LD) 8-Lead



882246  
Top View  
See NS Package Number LDC08A  
Pin 2 and pin 7 are fused to center DAP  
Pin 5 and 6 need to be tied together on PCB board

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

LM2940S, J, WG, T, MP	7100 ms	60V
LM2940CS, T	71 ms	45V
Internal Power Dissipation	(Note 2)	Internally Limited
Maximum Junction Temperature		150 C
Storage Temperature Range	65 C	7T <sub>J</sub> 7+150 C
Soldering Temperature (Note 3)		
TO-220 (T), Wave		260 C, 10s
TO-263 (S)		235 C, 30s

SOT-223 (MP)

260 C, 30s

LLP-8 (LD)

235 C, 30s

ESD Susceptibility (Note 4)

2 kV

**Operating Conditions** (Note 1)

Input Voltage		26V
Temperature Range		
LM2940T, LM2940S	40 C	7T <sub>J</sub> 7125 C
LM2940CT, LM2940CS	0 C	7T <sub>J</sub> 7125 C
LM2940IMP	40 C	7T <sub>A</sub> 785 C
LM2940J, LM2940WG	55 C	7T <sub>J</sub> 7125 C
LM2940LD	40 C	7T <sub>J</sub> 7125 C

**Electrical Characteristics**

V<sub>IN</sub> = V<sub>O</sub> + 5V, I<sub>O</sub> = 1A, C<sub>O</sub> F unless otherwise specified. Boldface limits apply over the entire operating temperature range of the indicated device. All other specifications apply for T<sub>A</sub> = T<sub>J</sub> = 25 C.

Output Voltage (V <sub>O</sub> )		5V			8V			Units
Parameter	Conditions	Typ	LM2940 Limit (Note 5)	LM2940/883 Limit (Note 6)	Typ	LM2940 Limit (Note 5)	LM2940/883 Limit (Note 6)	
Output Voltage	5 mA 7I <sub>O</sub> 71A	6.25V 7V <sub>IN</sub> 726V			9.4V 7V <sub>IN</sub> 726V			V <sub>MIN</sub> V <sub>MAX</sub>
		5.00	4.85/4.75 5.15/5.25	4.85/4.75 5.15/5.25	8.00	7.76/7.60 8.24/8.40	7.76/7.60 8.24/8.40	
Line Regulation	V <sub>O</sub> + 2V 7V <sub>IN</sub> 726V, I <sub>O</sub> = 5 mA	20	50	40/50	20	80	50/80	mV <sub>MAX</sub>
Load Regulation	50 mA 7I <sub>O</sub> 71A LM2940, LM2940/883 LM2940C	35	50/80	50/100	55	80/130	80/130	mV <sub>MAX</sub>
		35	50		55	80		
Output Impedance	100 mADC and 20 mArms, f <sub>O</sub> = 120 Hz	35		1000/1000	55		1000/1000	m Ω
Quiescent Current	V <sub>O</sub> + 2V 7V <sub>IN</sub> 726V, I <sub>O</sub> = 5 mA LM2940, LM2940/883 LM2940C	10	15/20	15/20	10	15/20	15/20	mA <sub>MAX</sub>
		10	15					
	V <sub>IN</sub> = V <sub>O</sub> + 5V, I <sub>O</sub> = 1A	30	45/60	50/60	30	45/60	50/60	mA <sub>MAX</sub>
Output Noise Voltage	10 Hz 100 kHz, I <sub>O</sub> = 5 mA	150		700/700	240		1000/1000	μV <sub>rms</sub>
Ripple Rejection	f <sub>O</sub> = 120 Hz, 1 V <sub>rms</sub> , I <sub>O</sub> = 100 mA LM2940 LM2940C	72	60/54		66	54/48		dB <sub>MIN</sub>
		72	60		66	54		
	f <sub>O</sub> = 1 kHz, 1 V <sub>rms</sub> , I <sub>O</sub> = 5 mA			60/50			54/48	dB <sub>MIN</sub>
Long Term Stability		20			32			mV/ 1000 Hr
Dropout Voltage	I <sub>O</sub> = 1A	0.5	0.8/1.0	0.7/1.0	0.5	0.8/1.0	0.7/1.0	V <sub>MAX</sub>
	I <sub>O</sub> = 100 mA	110	150/200	150/200	110	150/200	150/200	mV <sub>MAX</sub>

Output Voltage ( $V_O$ )		5V			8V			Units
Parameter	Conditions	Typ	LM2940 Limit (Note 5)	LM2940/883 Limit (Note 6)	Typ	LM2940 Limit (Note 5)	LM2940/883 Limit (Note 6)	
Short Circuit Current	(Note 7)	1.9	1.6	1.5/1.3	1.9	1.6	1.6/1.3	$A_{MIN}$
Maximum Line Transient	$R_O$ $\ddot{O}$ LM2940, T 7100 ms	75	60/60		75	60/60		$V_{MIN}$
	LM2940/883, T 720 ms			40/40			40/40	
	LM2940C, T 71 ms	55	45		55	45		
Reverse Polarity DC Input Voltage	$R_O$ $\ddot{O}$ LM2940, LM2940/883	30	15/ 15	15/ 15	30	15/ 15	15/ 15	$V_{MIN}$
	LM2940C	30	15		30	15		
Reverse Polarity Transient Input Voltage	$R_O$ $\ddot{O}$ LM2940, T 7100 ms	75	50/ 50		75	50/ 50		$V_{MIN}$
	LM2940/883, T 720 ms			45/ 45			45/ 45	
	LM2940C, T 71 ms	55	45/ 45					

## Electrical Characteristics

$V_{IN} = V_O + 5V$ ,  $I_O = 1A$ ,  $C_O$  Unless otherwise specified. Boldface limits apply over the entire operating temperature range of the indicated device. All other specifications apply for  $T_A = T_J = 25\text{ C}$ .

Output Voltage ( $V_O$ )		9V		10V		Units
Parameter	Conditions	Typ	LM2940 Limit (Note 5)	Typ	LM2940 Limit (Note 5)	
Output Voltage	5 mA $I_O$ 71A	10.5V $7V_{IN}$ 726V		11.5V $7V_{IN}$ 726V		$V_{MIN}$ $V_{MAX}$
		9.00	8.73/8.55	10.00	9.70/9.50	
			9.27/9.45		10.30/10.50	
Line Regulation	$V_O + 2V$ $7V_{IN}$ 726V, $I_O = 5\text{ mA}$	20	90	20	100	$mV_{MAX}$
Load Regulation	50 mA $I_O$ 71A LM2940 LM2940C	60	90/150	65	100/165	$mV_{MAX}$
		60	90			
Output Impedance	100 mADC and 20 mArms, $f_O = 120\text{ Hz}$	60		65		$m\ddot{O}$
Quiescent Current	$V_O + 2V$ $7V_{IN} < 26V$ , $I_O = 5\text{ mA}$ LM2940 LM2940C	10	15/20	10	15/20	$mA_{MAX}$
		10	15			
		$V_{IN} = V_O + 5V$ , $I_O = 1A$	30	45/60	30	
Output Noise Voltage	10 Hz 100 kHz, $I_O = 5\text{ mA}$	270		300		$\ddot{V}_{rms}$
Ripple Rejection	$f_O = 120\text{ Hz}$ , 1 $V_{rms}$ , $I_O = 100\text{ mA}$ LM2940 LM2940C	64	52/46	63	51/45	$dB_{MIN}$
		64	52			
Long Term Stability		34		36		$mV/$ 1000 Hr

Output Voltage ( $V_O$ )		9V		10V		Units
Parameter	Conditions	Typ	LM2940 Limit (Note 5)	Typ	LM2940 Limit (Note 5)	
Dropout Voltage	$I_O = 1A$	0.5	0.8/1.0	0.5	0.8/1.0	$V_{MAX}$
	$I_O = 100\text{ mA}$	110	150/200	110	150/200	$mV_{MAX}$
Short Circuit Current	(Note 7)	1.9	1.6	1.9	1.6	$A_{MIN}$
Maximum Line Transient	$R_O$ $\ddot{O}$ $T = 7100\text{ ms}$ LM2940 LM2940C	75 55	60/60 45	75	60/60	$V_{MIN}$
Reverse Polarity DC Input Voltage	$R_O$ $\ddot{O}$ LM2940 LM2940C	30 30	15/ 15 15	30	15/ 15	$V_{MIN}$
Reverse Polarity Transient Input Voltage	$R_O$ $\ddot{O}$ $T = 7100\text{ ms}$ LM2940 LM2940C	75 55	50/ 50 45/ 45	75	50/ 50	$V_{MIN}$

## Electrical Characteristics

$V_{IN} = V_O + 5V$ ,  $I_O = 1A$ ,  $C_O$   $F$  unless otherwise specified. Boldface limits apply over the entire operating temperature range of the indicated device. All other specifications apply for  $T_A = T_J = 25\text{ C}$ .

Output Voltage ( $V_O$ )		12V			15V			Units
Parameter	Conditions	Typ	LM2940 Limit (Note 5)	LM2940/833 Limit (Note 6)	Typ	LM2940 Limit (Note 5)	LM2940/833 Limit (Note 6)	
Output Voltage	$5\text{ mA}$ $7I_O$ $71A$	<b>13.6V</b> $7V_{IN}$ <b>726V</b>			<b>16.75V</b> $7V_{IN}$ <b>726V</b>			$V_{MIN}$
		12.00	11.64/11.40 12.36/12.60	11.64/11.40 12.36/12.60	15.00	14.55/14.25 15.45/15.75	14.55/14.25 15.45/15.75	$V_{MAX}$
Line Regulation	$V_O + 2V$ $7V_{IN}$ $726V$ , $I_O = 5\text{ mA}$	20	120	75/120	20	150	95/150	$mV_{MAX}$
Load Regulation	$50\text{ mA}$ $7I_O$ $71A$ LM2940, LM2940/883 LM2940C	55	120/200	120/190			150/240	$mV_{MAX}$
		55	120		70	150		
Output Impedance	100 mADC and 20 mArms, $f_O = 120\text{ Hz}$	80		1000/1000	100		1000/1000	$m\ddot{O}$
Quiescent Current	$V_O + 2V$ $7V_{IN}$ $726V$ , $I_O = 5\text{ mA}$ LM2940, LM2940/883 LM2940C	10	15/20	15/20			15/20	$mA_{MAX}$
		10	15		10	15		
	$V_{IN} = V_O + 5V$ , $I_O = 1A$	30	45/60	50/60	30	45/60	50/60	$mA_{MAX}$
Output Noise Voltage	10 Hz 100 kHz, $I_O = 5\text{ mA}$	360		1000/1000	450		1000/1000	$\ddot{v}_{rms}$

Output Voltage (V <sub>O</sub> )		12V			15V			Units
Parameter	Conditions	Typ	LM2940 Limit (Note 5)	LM2940/833 Limit (Note 6)	Typ	LM2940 Limit (Note 5)	LM2940/833 Limit (Note 6)	
Ripple Rejection	f <sub>O</sub> = 120 Hz, 1 V <sub>rms</sub> , I <sub>O</sub> = 100 mA							dB <sub>MIN</sub>
	LM2940	66	54/48					
	LM2940C	66	54		64	52		
	f <sub>O</sub> = 1 kHz, 1 V <sub>rms</sub> , I <sub>O</sub> = 5 mA			52/46			48/42	dB <sub>MIN</sub>
Long Term Stability		48			60			mV/ 1000 Hr
Dropout Voltage	I <sub>O</sub> = 1A	0.5	0.8/1.0	0.7/1.0	0.5	0.8/1.0	0.7/1.0	V <sub>MAX</sub>
	I <sub>O</sub> = 100 mA	110	150/200	150/200	110	150/200	150/200	mV <sub>MAX</sub>
Short Circuit Current	(Note 7)	1.9	1.6	1.6/1.3	1.9	1.6	1.6/1.3	A <sub>MIN</sub>
Maximum Line Transient	R <sub>O</sub> Ö							V <sub>MIN</sub>
	LM2940, T 7100 ms	75	60/60					
	LM2940/883, T 720 ms			40/40			40/40	
	LM2940C, T 71 ms	55	45		55	45		
Reverse Polarity DC Input Voltage	R <sub>O</sub> Ö							V <sub>MIN</sub>
	LM2940, LM2940/883	30	15/ 15	15/ 15			15/ 15	
	LM2940C	30	15		30	15		
Reverse Polarity Transient Input Voltage	R <sub>O</sub> Ö							V <sub>MIN</sub>
	LM2940, T 7100 ms	75	50/ 50					
	LM2940/883, T 720 ms			45/ 45			45/ 45	
	LM2940C, T 71 ms	55	45/ 45		55	45/ 45		

## Thermal Performance

Thermal Resistance Junction-to-Case, $\theta_{JC}$	3-Lead TO-220	4		C/W
	3-Lead TO-263	4		
Thermal Resistance Junction-to-Ambient, $\theta_{JA}$	3-Lead TO-220 (Note 2)	60		C/W
	3-Lead TO-263 (Note 2)	80		
	SOT-223(Note 2)	174		
	8-Lead LLP (Note 2)	35		

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Conditions are conditions under which the device functions but the specifications might not be guaranteed. For guaranteed specifications and test conditions see the Electrical Characteristics.

Note 2: The maximum allowable power dissipation is a function of the maximum junction temperature, T<sub>J</sub>, the junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature, T<sub>A</sub>. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. The value of  $\theta_{JA}$  (for devices in still air with no heatsink) is 60 C/W for the TO-220 package, 80 C/W for the TO-263 package, and 174 C/W for the SOT-223 package. The effective value of  $\theta_{JA}$  can be reduced by using a heatsink (see Application Hints for specific information on heatsinking). The value of  $\theta_{JA}$  for the LLP package is specifically dependent on PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the LLP package, refer to Application Note AN-1187. It is recommended that 6 vias be placed under the center pad to improve thermal performance.

Note 3: Refer to JEDEC J-STD-020C for surface mount device (SMD) package reflow profiles and conditions. Unless otherwise stated, the temperature and time are for Sn-Pb (STD) only.

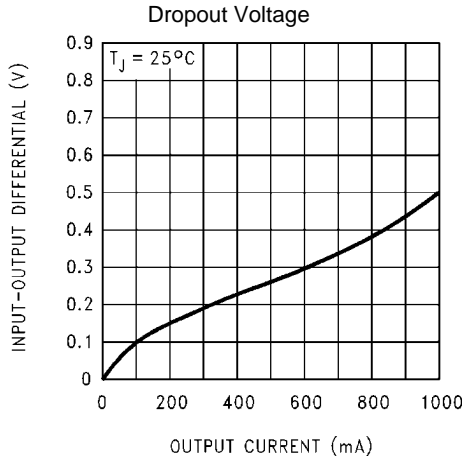
Note 4: ESD rating is based on the human body model, 100 pF discharged through 1.5 k Ω

Note 5: All limits are guaranteed at T<sub>A</sub> = T<sub>J</sub> = 25 C only (standard typeface) or over the entire operating temperature range of the indicated device (boldface type). All limits at T<sub>A</sub> = T<sub>J</sub> = 25 C are 100% production tested. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control methods.

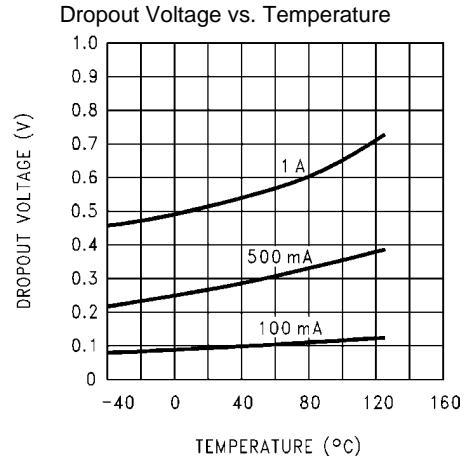
Note 6: All limits are guaranteed at T<sub>A</sub> = T<sub>J</sub> = 25 C only (standard typeface) or over the entire operating temperature range of the indicated device (boldface type). All limits are 100% production tested and are used to calculate Outgoing Quality Levels.

Note 7: Output current will decrease with increasing temperature but will not drop below 1A at the maximum specified temperature.

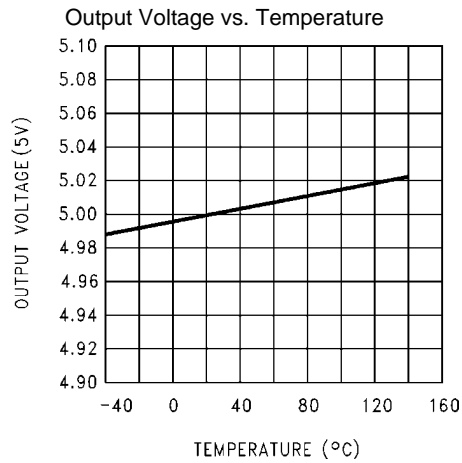
# Typical Performance Characteristics



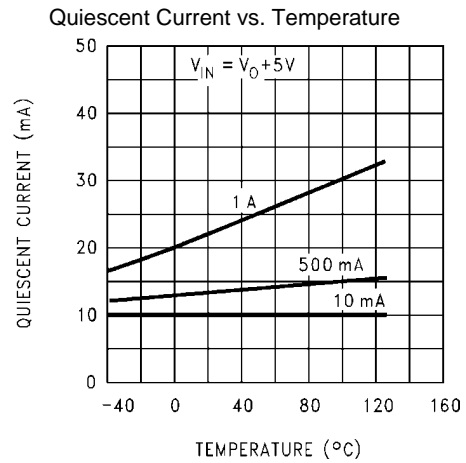
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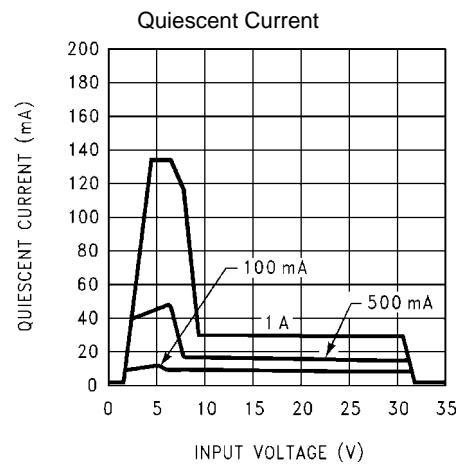
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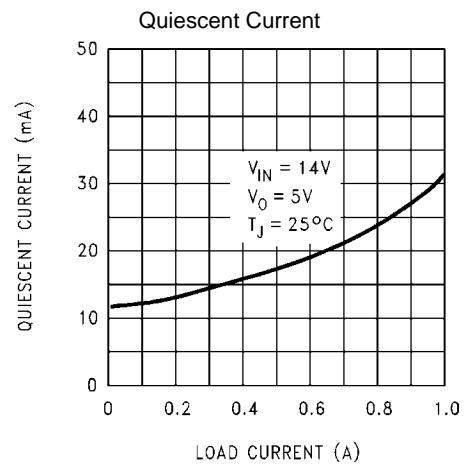
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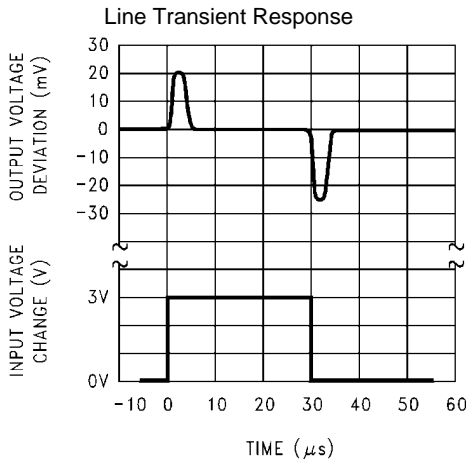


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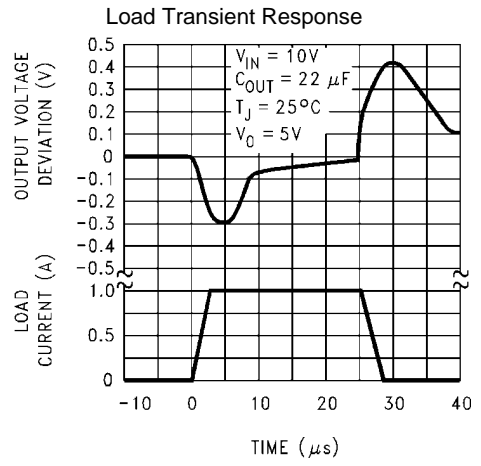


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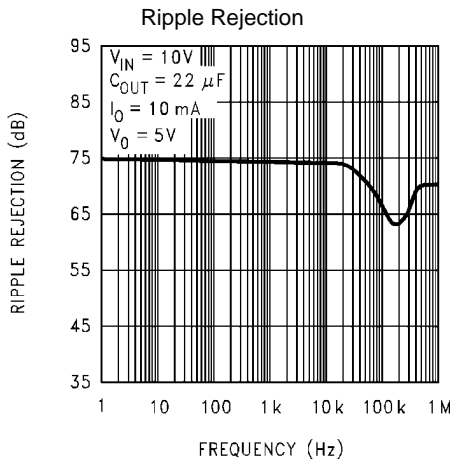




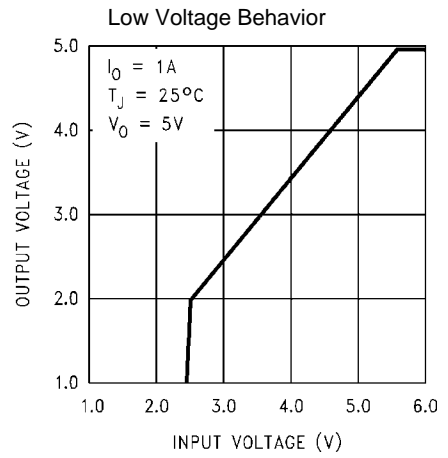
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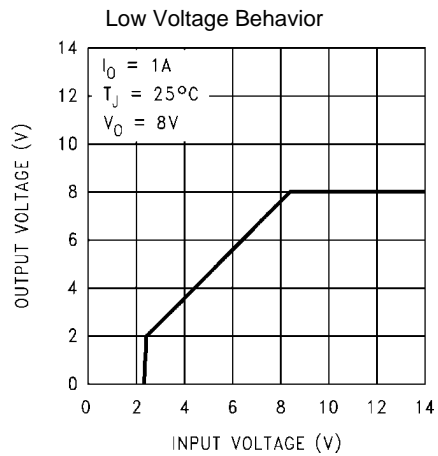
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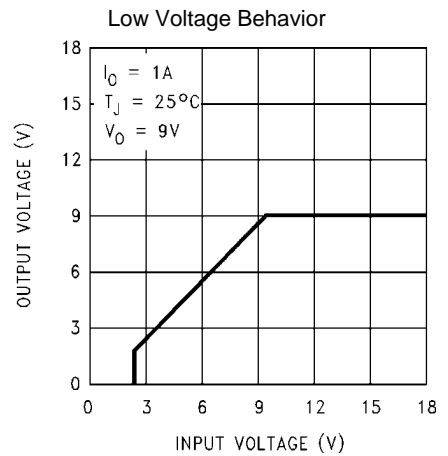
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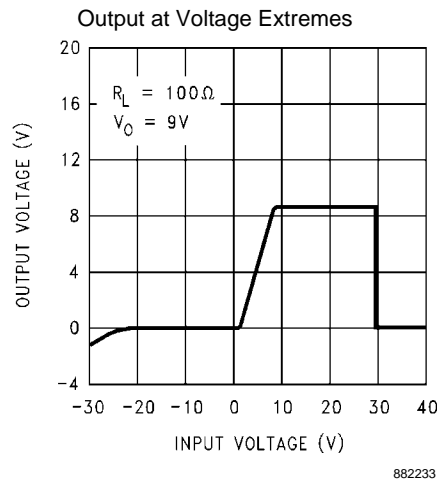
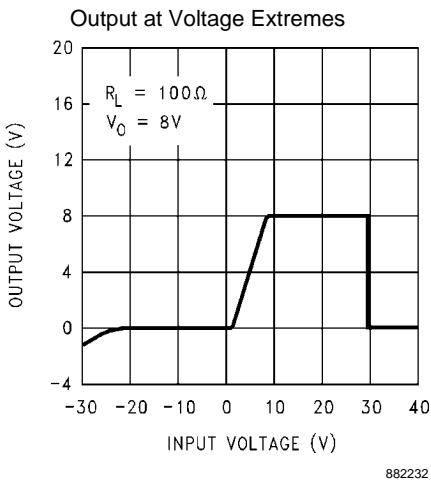
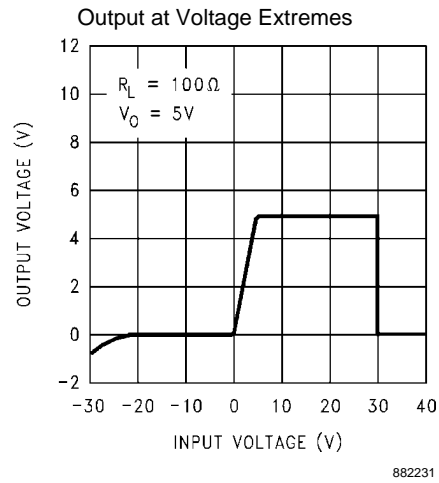
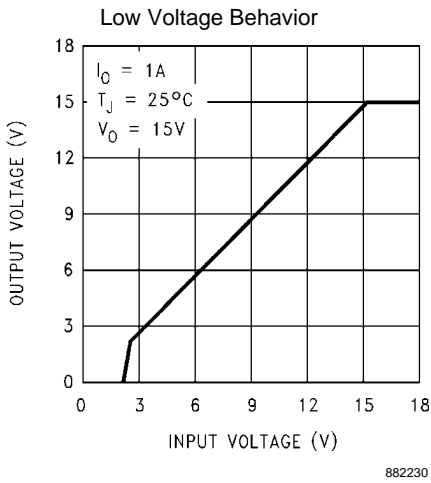
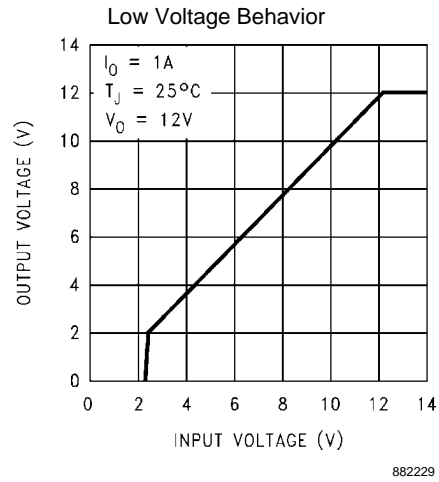
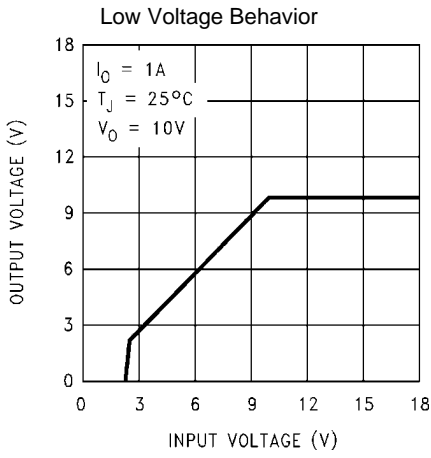
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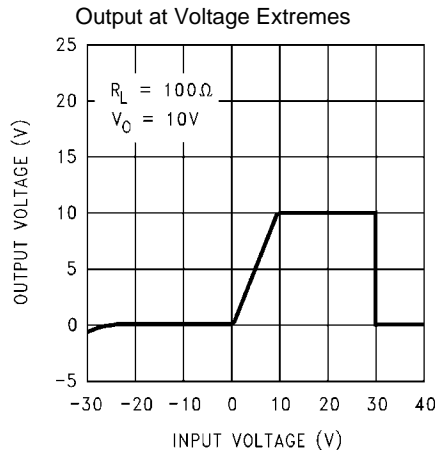


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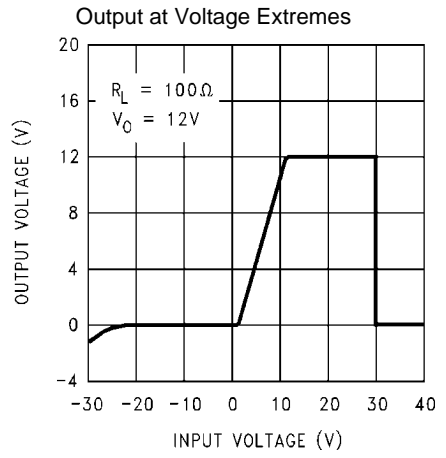


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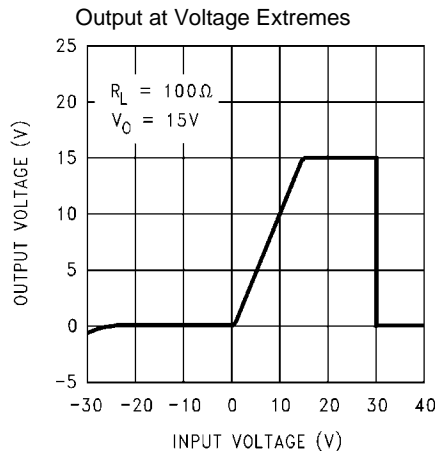




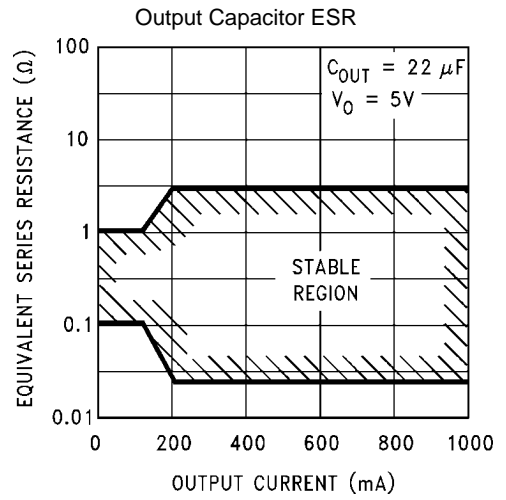
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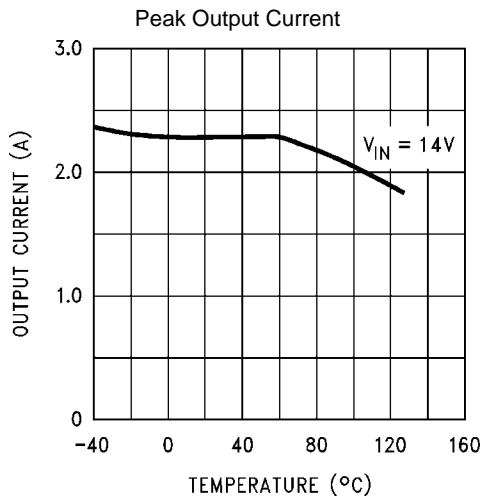
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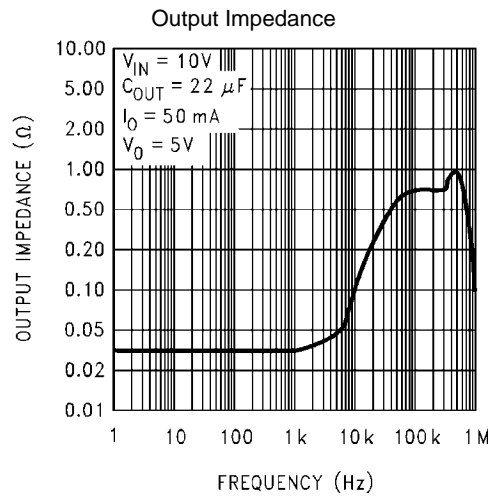
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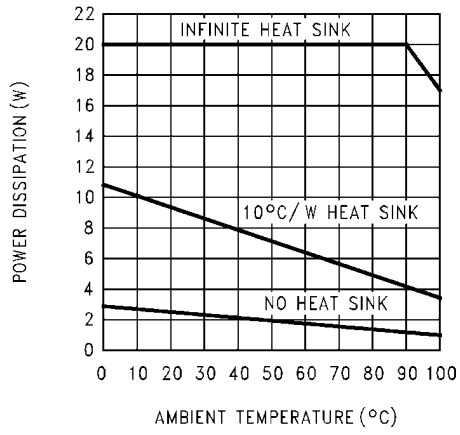


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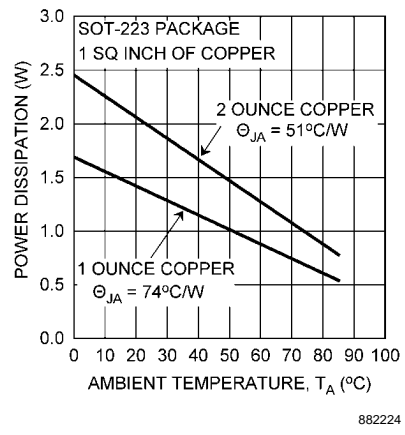
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Maximum Power Dissipation (TO-220)



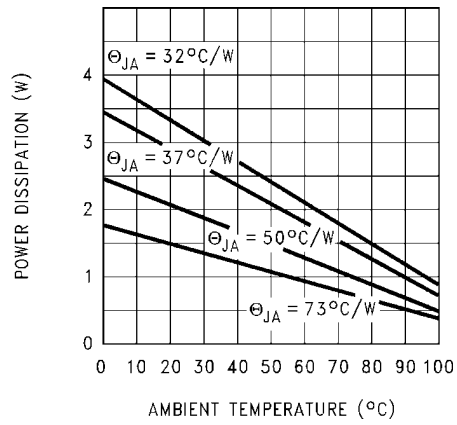
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Maximum Power Dissipation (SOT-223)



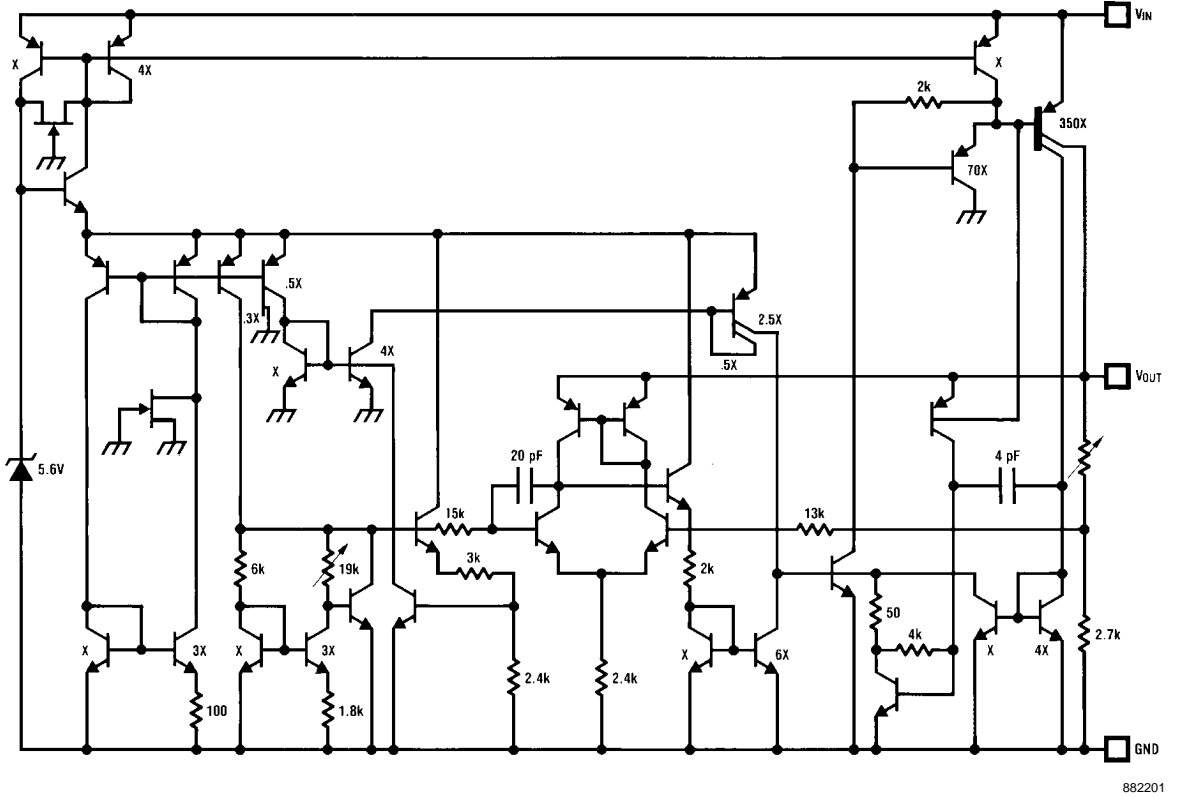
882224

Maximum Power Dissipation (TO-263)



882210

# Equivalent Schematic Diagram



# Application Information

## EXTERNAL CAPACITORS

The output capacitor is critical to maintaining regulator stability, and must meet the required conditions for both ESR (Equivalent Series Resistance) and minimum amount of capacitance.

### MINIMUM CAPACITANCE:

The minimum output capacitance required to maintain stability is 22 μF (this value may be increased without limit). Larger values of output capacitance will give improved transient response.

### ESR LIMITS:

The ESR of the output capacitor will cause loop instability if it is too high or too low. The acceptable range of ESR plotted versus load current is shown in the graph below. It is essential that the output capacitor meet these requirements, or oscillations can result.

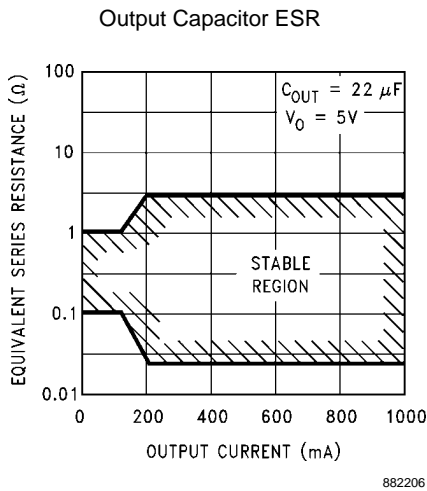


FIGURE 1. ESR Limits

It is important to note that for most capacitors, ESR is specified only at room temperature. However, the designer must ensure that the ESR will stay inside the limits shown over the entire operating temperature range for the design.

For aluminum electrolytic capacitors, ESR will increase by about 30X as the temperature is reduced from 25 C to 40 C. This type of capacitor is not well-suited for low temperature operation.

Solid tantalum capacitors have a more stable ESR over temperature, but are more expensive than aluminum electrolytics. A cost-effective approach sometimes used is to parallel an aluminum electrolytic with a solid Tantalum, with the total capacitance split about 75/25% with the Aluminum being the larger value.

If two capacitors are paralleled, the effective ESR is the parallel of the two individual values. The "flatter" ESR of the Tantalum will keep the effective ESR from rising as quickly at low temperatures.

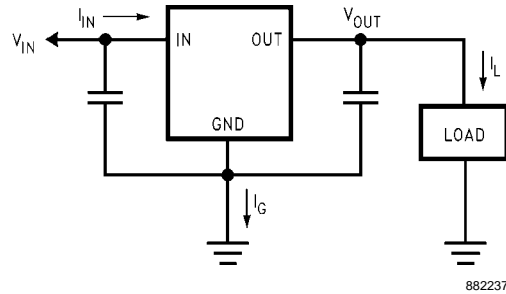
## HEATSINKING

A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible operating conditions, the junction

temperature must be within the range specified under Absolute Maximum Ratings.

To determine if a heatsink is required, the power dissipated by the regulator, P<sub>D</sub>, must be calculated.

The figure below shows the voltages and currents which are present in the circuit, as well as the formula for calculating the power dissipated in the regulator:



$$I_{IN} = I_L + I_G$$

$$P_D = (V_{IN} - V_{OUT}) I_L + (V_{IN}) I_G$$

FIGURE 2. Power Dissipation Diagram

The next parameter which must be calculated is the maximum allowable temperature rise, T<sub>R(MAX)</sub>. This is calculated by using the formula:

$$T_{R(MAX)} = T_{J(MAX)} - T_{A(MAX)}$$

where: T<sub>J(MAX)</sub> is the maximum allowable junction temperature, which is 125 C for commercial grade parts.

T<sub>A(MAX)</sub> is the maximum ambient temperature which will be encountered in the application.

Using the calculated values for T<sub>R(MAX)</sub> and P<sub>D</sub>, the maximum allowable value for the junction-to-ambient thermal resistance, θ<sub>JA</sub>, can now be found:

$$\theta_{JA} = T_{R(MAX)} / P_D$$

**IMPORTANT:** If the maximum allowable value for θ<sub>JA</sub> is found to be 853 C/W for the TO-220 package, 880 C/W for the TO-263 package, or 8174 C/W for the SOT-223 package, no heatsink is needed since the package alone will dissipate enough heat to satisfy these requirements.

If the calculated value for θ<sub>JA</sub> falls below these limits, a heatsink is required.

## HEATSINKING TO-220 PACKAGE PARTS

The TO-220 can be attached to a typical heatsink, or secured to a copper plane on a PC board. If a copper plane is to be used, the values of θ<sub>JA</sub> will be the same as shown in the next section for the TO-263.

If a manufactured heatsink is to be selected, the value of heatsink-to-ambient thermal resistance, θ<sub>HA</sub>, must first be calculated:

$$\theta_{HA} = \theta_{JA} - \theta_{JC} - \theta_{CH} - \theta_{CA}$$

Where: θ<sub>JC</sub> is defined as the thermal resistance from the junction to the surface of the case. A value of 3 C/W can be assumed for θ<sub>JC</sub> for this calculation.

$\theta_{CH}$  is defined as the thermal resistance between the case and the surface of the heatsink. The value of  $\theta_{CH}$  will vary from about 1.5 C/W to about 2.5 C/W (depending on method of attachment, insulator, etc.). If the exact value is unknown, 2 C/W should be assumed for  $\theta_{CH}$ .

When a value for  $\theta_{HA}$  is found using the equation shown, a heatsink must be selected that has a value that is less than or equal to this number.

$\theta_{HA}$  is specified numerically by the heatsink manufacturer in the catalog, or shown in a curve that plots temperature rise vs power dissipation for the heatsink.

**HEATSINKING TO-263 PACKAGE PARTS**

The TO-263 (S<sup>0</sup>) package uses a copper plane on the PCB and the PCB itself as a heatsink. To optimize the heat sinking ability of the plane and PCB, solder the tab of the package to the plane.

Figure 3 shows for the TO-263 the measured values of  $\theta_{JA}$  for different copper area sizes using a typical PCB with 1 ounce copper and no solder mask over the copper area used for heatsinking.

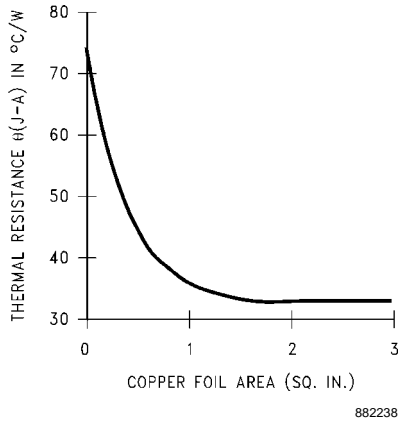


FIGURE 3.  $\theta_{JA}$  vs. Copper (1 ounce) Area for the TO-263 Package

As shown in the figure, increasing the copper area beyond 1 square inch produces very little improvement. It should also be observed that the minimum value of  $\theta_{JA}$  for the TO-263 package mounted to a PCB is 32 C/W.

As a design aid, Figure 4 shows the maximum allowable power dissipation compared to ambient temperature for the TO-263 device. This assumes a  $\theta_{JA}$  of 35 C/W for 1 square inch of 1 ounce copper and a maximum junction temperature ( $T_J$ ) of 125 C.

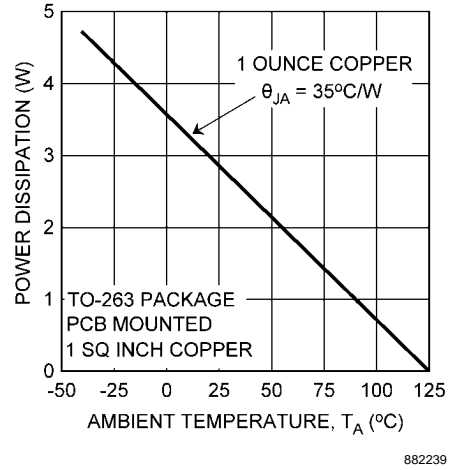


FIGURE 4. Maximum Power Dissipation vs.  $T_A$  for the TO-263 Package

**HEATSINKING SOT-223 PACKAGE PARTS**

The SOT-223 (MP<sup>0</sup>) packages use a copper plane on the PCB and the PCB itself as a heatsink. To optimize the heat sinking ability of the plane and PCB, solder the tab of the package to the plane.

Figure 5 and Figure 6 show the information for the SOT-223 package. Figure 6 assumes a  $\theta_{JA}$  of 74 C/W for 1 square inch of 1 ounce copper and 51 C/W for 1 square inch of 2 ounce copper, with a maximum ambient temperature ( $T_A$ ) of 85 C and a maximum junction temperature ( $T_J$ ) of 125 C.

For techniques for improving the thermal resistance and power dissipation for the SOT-223 package, please refer to Application Note AN-1028.

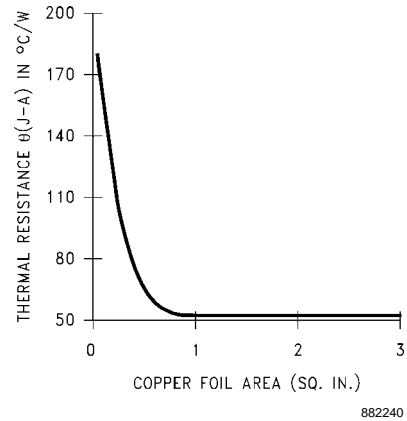


FIGURE 5.  $\theta_{JA}$  vs. Copper (2 ounce) Area for the SOT-223 Package

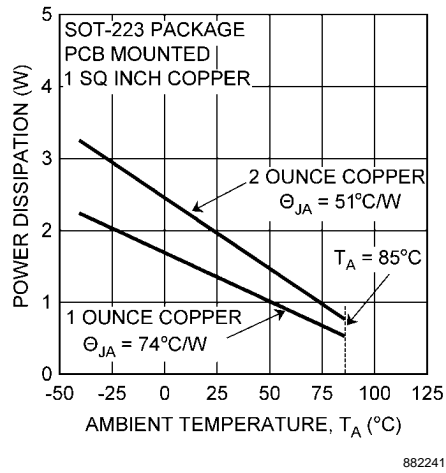


FIGURE 6. Maximum Power Dissipation vs.  $T_A$  for the SOT-223 Package

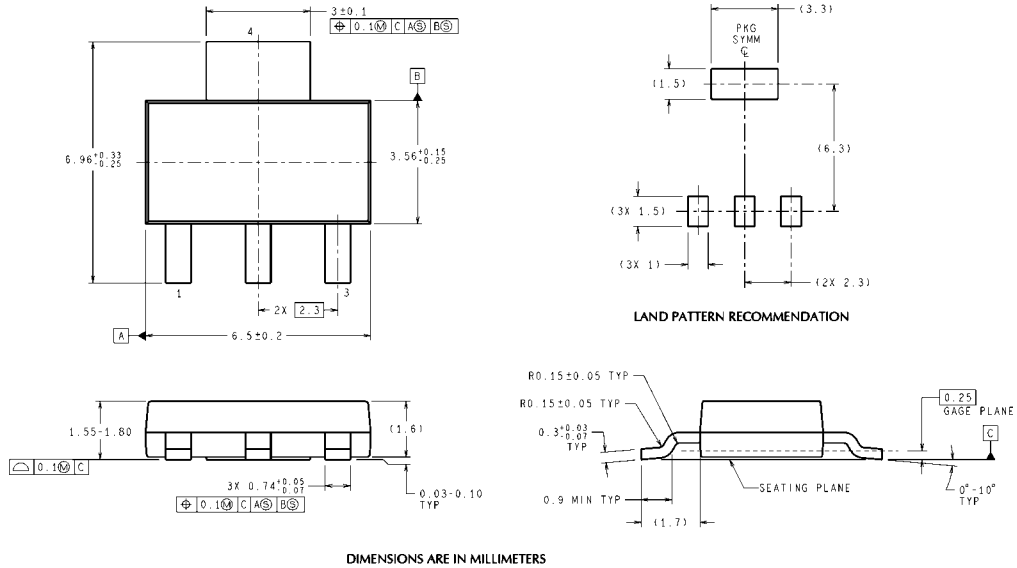
#### HEATSINKING LLP PACKAGE PARTS

The value of  $\hat{\theta}_{JA}$  for the LLP package is specifically dependent on PCB trace area, trace material, and the number of layers and thermal vias. It is recommended that a minimum of 6 thermal vias be placed under the center pad to improve thermal performance.

For techniques for improving the thermal resistance and power dissipation for the LLP package, please refer to Application Note AN-1187.

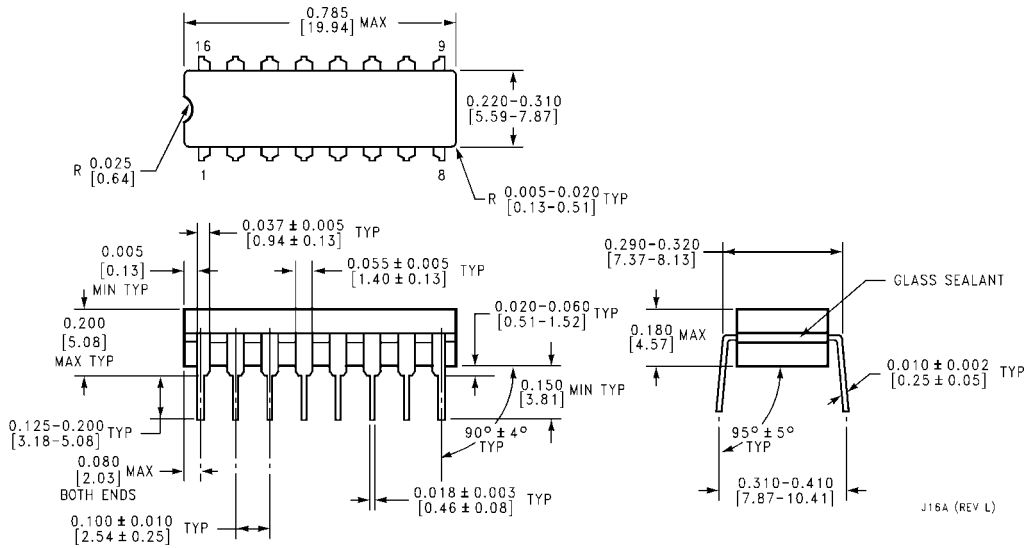


Physical Dimensions inches (millimeters) unless otherwise noted

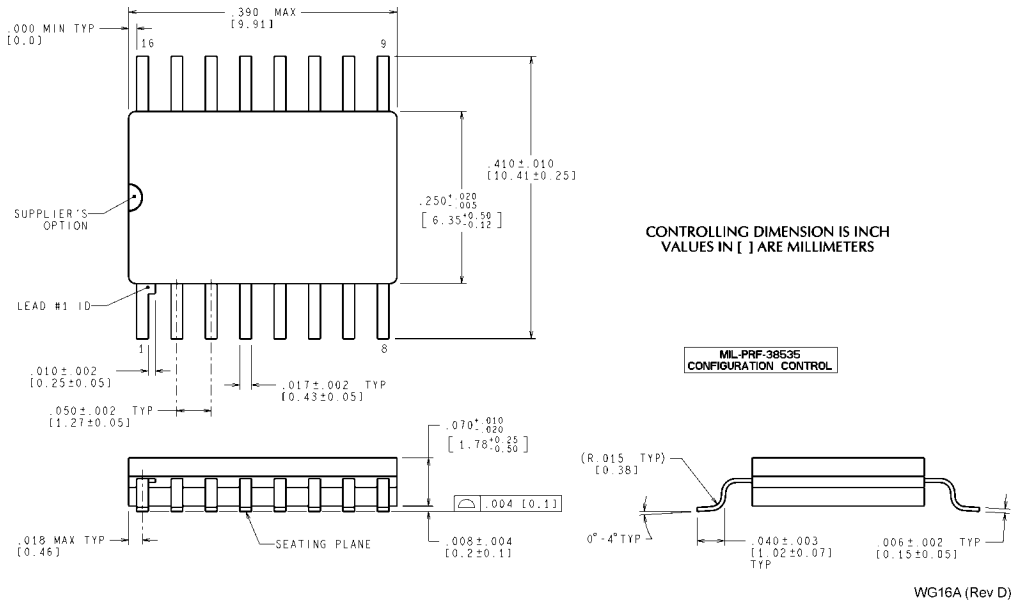


MP04A (Rev B)

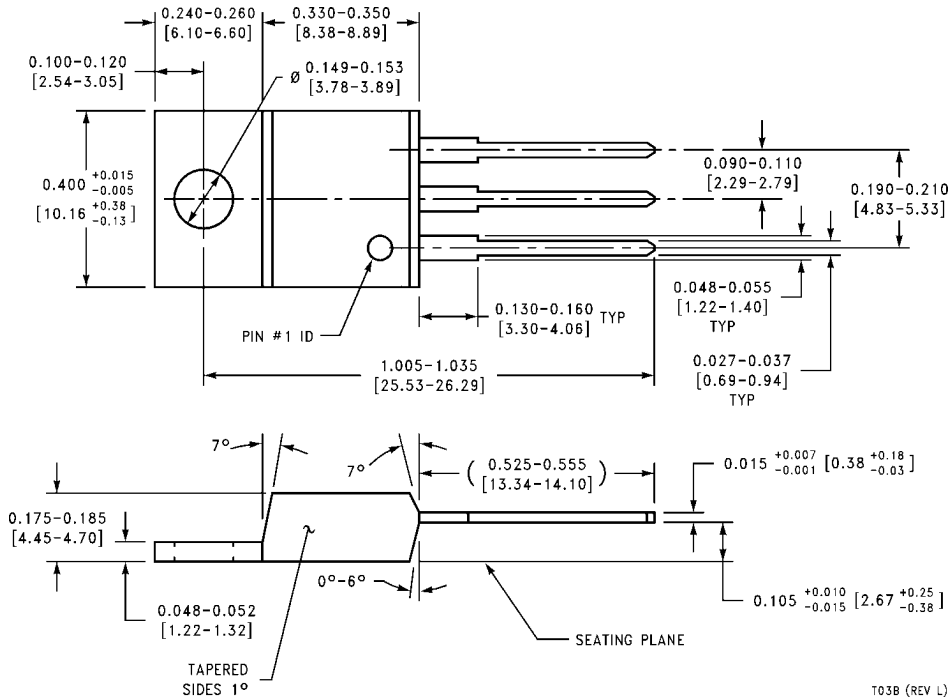
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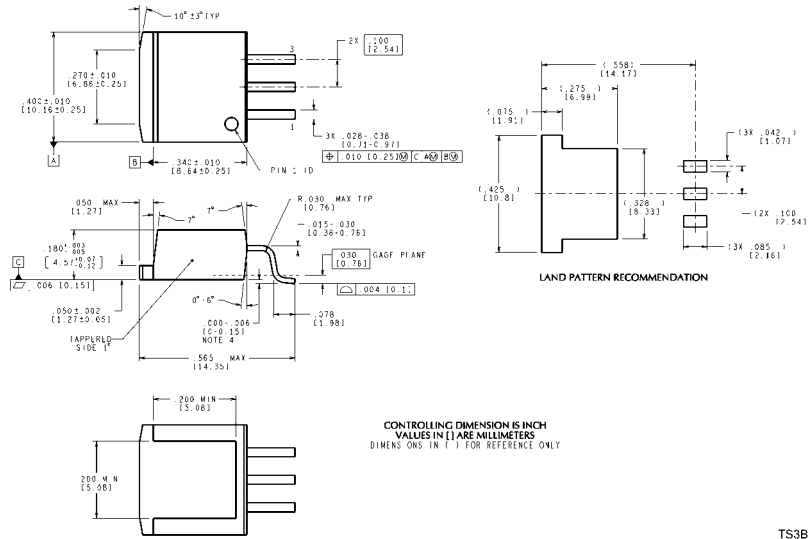
16 Lead Dual-in-Line Package (J)  
 See NS Package Number J16A



16 Lead Surface Mount Package (WG)  
See NS Package Number WG16A

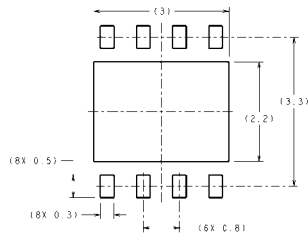


3-Lead TO-220 Plastic Package (T)  
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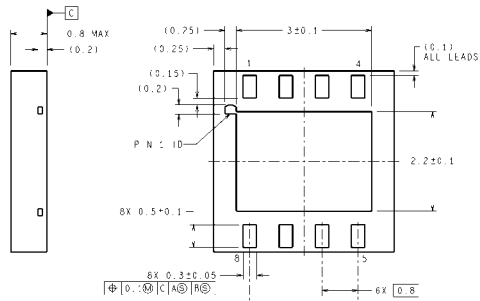
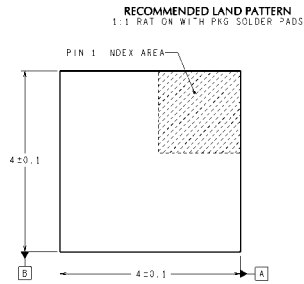


3-Lead TO-263 Surface Mount Package (MP)  
NS Package Number TS3B

TS3B (Rev F)



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LDC08A (Rev B)

8-Lead LLP  
Order Number LM2940LD-5.0, LM2940LD-8.0,  
LM2940LD-9.0, LM2940LD-10,  
LM2940LD-12 or LM2940LD-15  
NS Package Number LDC08A

# Notes

LM2940/LM2940C

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