PHE13005

Silicon diffused power transistor

Rev.01 - 30 March 2018 Product data sheet

1. General description

High voltage, high speed NPN planar-passivated power switching transistor in a SOT78 plastic package intended for use in high frequency electronic lighting ballast applications

2. Features and benefits

- Fast switching
- High voltage capability of 700 V
- Low thermal resistance

3. Applications

- Electronic lighting ballasts

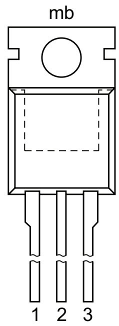
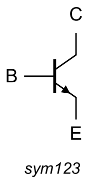
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Values		Unit
Absolute maximum rating						
V_{CESM}	peak collector-emitter voltage	V_{BE} = 0 V		700		V
I_C	collector current (DC)	DC; Fig. 1; Fig. 2; Fig. 4		4		A
P_{tot}	total power dissipation	T_{mb} ≤ 25 °C; Fig. 3		75		W
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Static characteristics						
h_{FE}	DC current gain	I_C = 1 A; V_{CE} = 5 V; T_{mb} = 25 °C; Fig. 11	12	20	40	
		I_C = 2 A; V_{CE} = 5 V; T_{mb} = 25 °C; Fig. 11	10	17	28	

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	B	base		
2	C	collector		
3	E	emitter		
mb	C	mounting base; connected to collector		

6. Ordering information

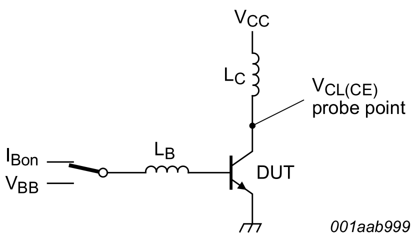
Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PHE13005	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

7. Limiting values

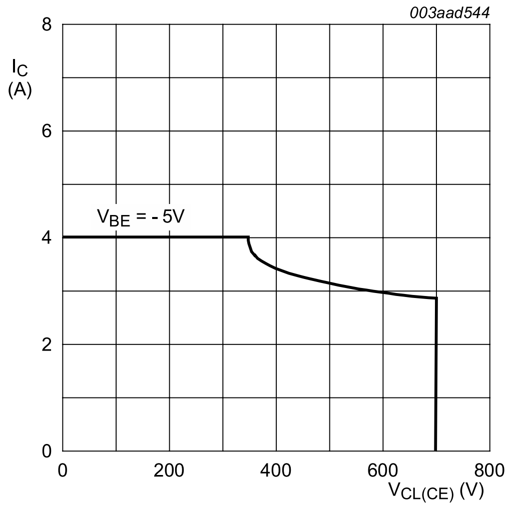
Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Values	Unit
V_{CESM}	peak collector-emitter voltage	V_{BE} = 0 V	700	V
V_{CBO}	collector-base voltage	I_E = 0 A	700	V
V_{CEO}	collector-emitter voltage	I_B = 0 A	400	V
I_C	collector current	DC; Fig. 1; Fig. 2; Fig. 4	4	A
I_{CM}	peak collector current		8	A
I_B	base current	DC	2	A
I_{BM}	peak base current		4	A
P_{tot}	total power dissipation	T_{mb} ≤ 25 °C; Fig. 3	75	W
T_{stg}	storage temperature		-65 to 150	°C
T_j	junction temperature		150	°C
V_{EBO}	emitter-base voltage	I_C = 0 A	9	V



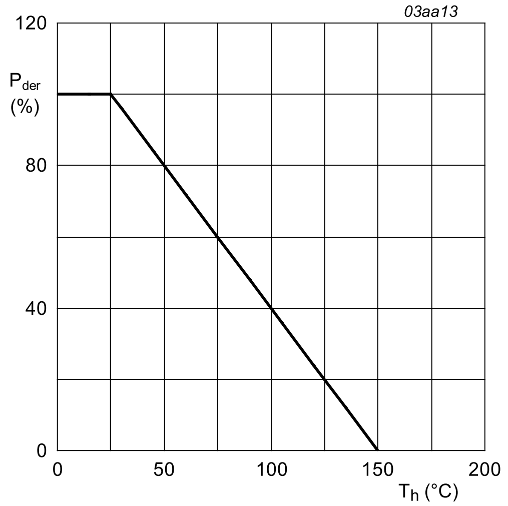
$V_{CL(CE)}$ ≤ 1000V; V_{CC} = 150 V; V_{BB} = -5 V;
L_C = 200 µH; L_B = 1 µH

Fig. 1. Test circuit for reverse bias safe operating area



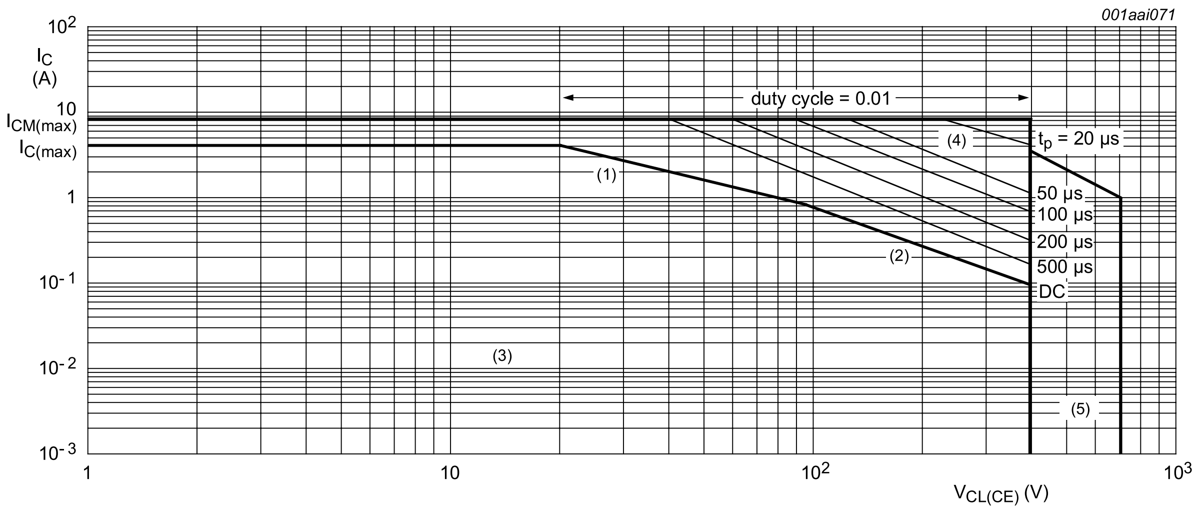
T_j ≤ $T_{j\,(max)}$ °C

Fig. 2. Reverse bias safe operating area



$$P_{der}(\%) = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\%$$

Fig. 3. Normalized total power dissipation as a function of heatsink temperature



$T_h \leq 25$ °C

Mounted with heatsink compound and (30 ± 5) N force on the centre of the envelope

(1) P_{tot} maximum and P_{tot} peak maximum lines

(2) Second breakdown limits

(3) Region of permissible DC operation

(4) Extension of operating region for repetitive pulse operation

(5) Extension of operating region during turn-on in single transistor converters provided that $R_{BE} \leq 100\ \Omega$ and $t_p \leq 0.6$ µs

Fig. 4. Forward bias safe operating area

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	-	1.67	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		-	60	-	K/W

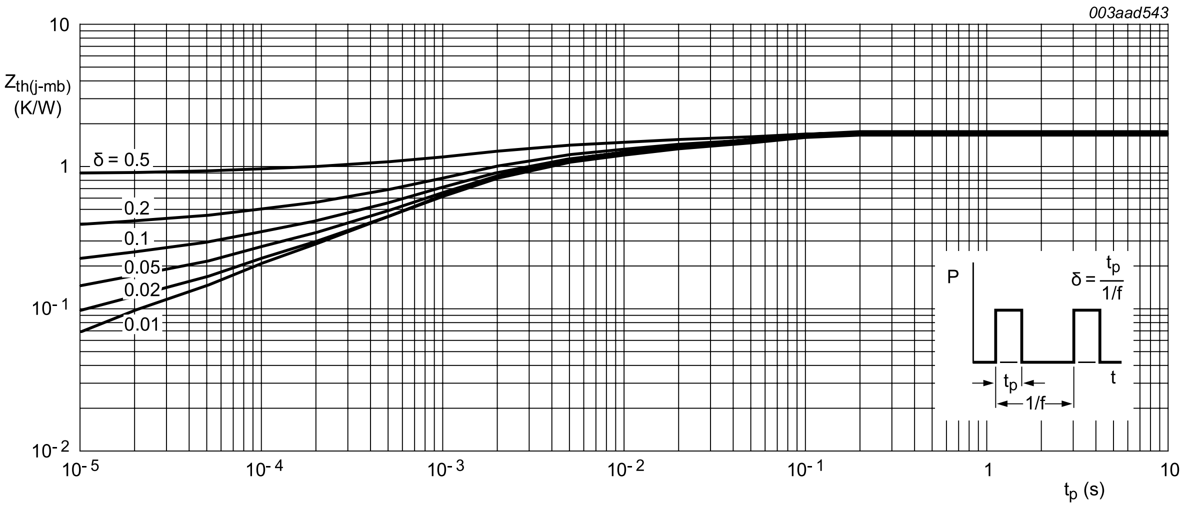


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

9. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{CES}	collector-emitter cut-off current	V_{BE} = -1.5 V; V_{CE} = 700 V; T_{mb} = 25 °C		-	-	1	mA
		V_{BE} = -1.5 V; V_{CE} = 700 V; T_j = 125 °C		-	-	5	mA
I_{CBO}	collector-base cut-off current	V_{CB} = 700 V; I_E = 0 A; T_{mb} = 25 °C		-	-	1	mA
I_{CEO}	collector-emitter cut-off current	V_{CEO} = 400 V; I_B = 0 A; T_{mb} = 25 °C		-	-	0.1	mA
I_{EBO}	emitter-base cut-off current	V_{EB} = 9 V; I_C = 0 A; T_{mb} = 25 °C		-	-	1	mA
V_{CEOsus}	collector-emitter sustaining voltage	I_B = 0 A; I_C = 10 mA; L_C = 25 mH; T_{mb} = 25 °C; Fig. 6; Fig. 7		400	-	-	V
V_{CEsat}	collector-emitter saturation voltage	I_C = 1.0 A; I_B = 0.2 A; T_{mb} = 25 °C; Fig. 8; Fig. 9		-	0.1	0.5	V
		I_C = 2.0 A; I_B = 0.5 A; T_{mb} = 25 °C; Fig. 8; Fig. 9		-	0.2	0.6	V
		I_C = 4.0 A; I_B = 1.0 A; T_{mb} = 25 °C; Fig. 8; Fig. 9		-	0.3	1	V
V_{BEsat}	base-emitter saturation voltage	I_C = 1.0 A; I_B = 0.2 A; T_{mb} = 25 °C; Fig. 10		-	0.85	1.2	V
		I_C = 2.0 A; I_B = 0.5 A; T_{mb} = 25 °C; Fig. 10		-	0.92	1.6	V
h_{FE}	DC current gain	I_C = 1 A; V_{CE} = 5 V; T_{mb} = 25 °C; Fig. 11		12	20	40	
		I_C = 2 A; V_{CE} = 5 V; T_{mb} = 25 °C; Fig. 11		10	17	28	
Dynamic characteristics							
t_s	storage time	I_C = 2 A; I_{Bon} = 0.4 A; I_{Boff} = -0.4 A; R_L = 75 Ω; T_{mb} = 25 °C; resistive load; Fig. 12; Fig. 13		-	2.7	4	µs
		I_C = 2 A; I_{Bon} = 0.4 A; V_{BB} = -5 V; L_B = 1 µH; T_{mb} = 25 °C; inductive load; Fig. 14; Fig. 15		-	1.2	2	µs
		I_C = 2 A; I_{Bon} = 0.4 A; V_{BB} = -5 V; L_B = 1 µH; T_{mb} = 100 °C; inductive load; Fig. 14; Fig. 15		-	1.4	4	µs
t_f	fall time	I_C = 2 A; I_{Bon} = 0.4 A; I_{Boff} = -0.4 A; R_L = 75 Ω; T_{mb} = 25 °C; resistive load; Fig. 12; Fig. 13		-	0.3	0.9	µs
		I_C = 2 A; I_{Bon} = 0.4 A; V_{BB} = -5 V; L_B = 1 µH; T_{mb} = 25 °C; inductive load; Fig. 14; Fig. 15		-	0.1	0.5	µs
		I_C = 2 A; I_{Bon} = 0.4 A; V_{BB} = -5 V; L_B = 1 µH; T_{mb} = 100 °C; inductive load; Fig. 14; Fig. 15		-	0.16	0.9	µs

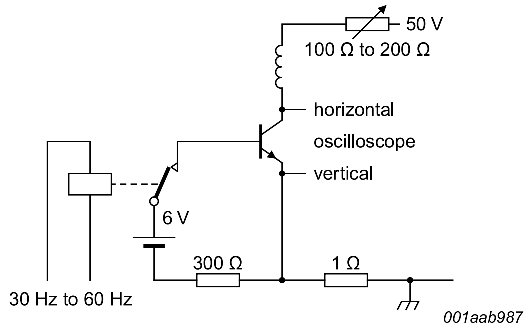


Fig. 6. Test circuit for collector-emitter sustaining voltage

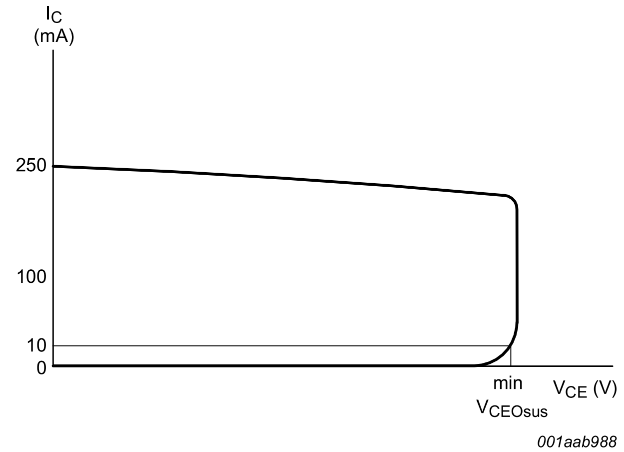


Fig. 7. Oscilloscope display for collector-emitter sustaining voltage test waveform

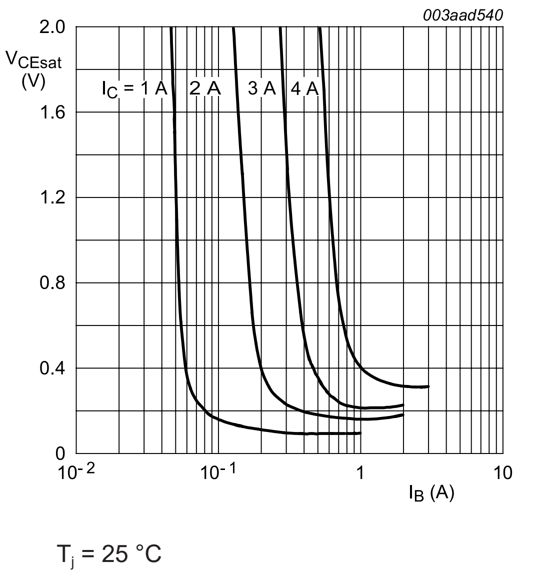


Fig. 8. Collector-emitter saturation voltage; typical values

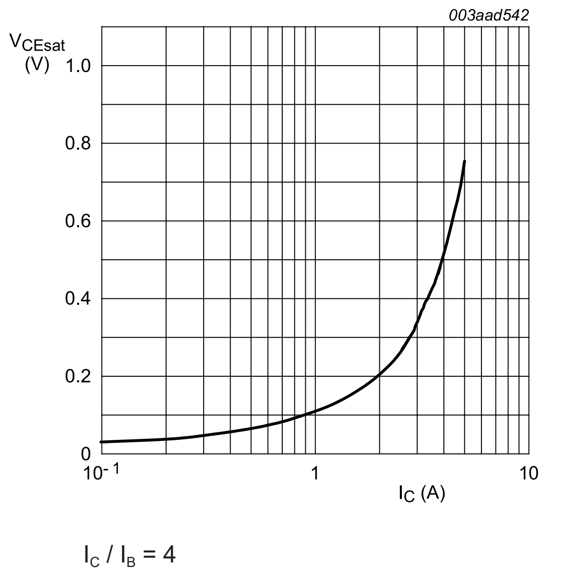
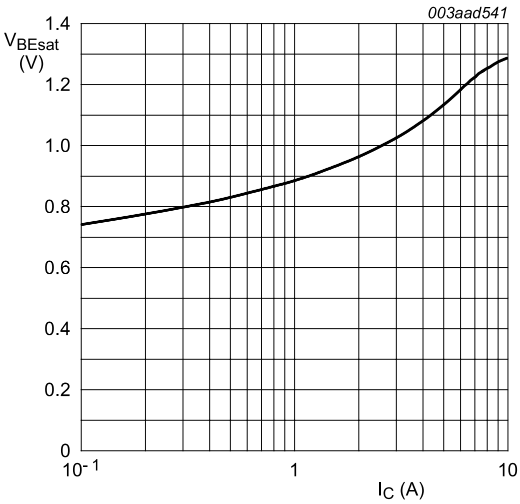
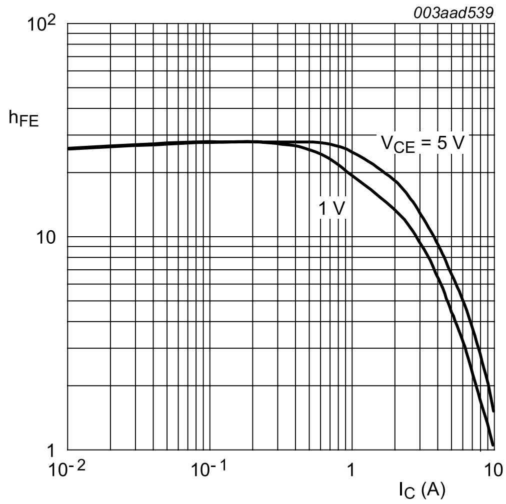


Fig. 9. Collector-emitter saturation voltage as a function of collector current; typical values



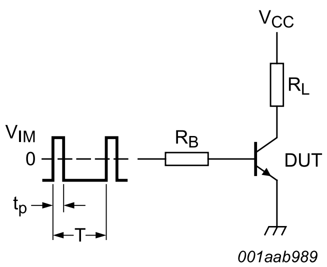
I_C / I_B = 4

Fig. 10. Base-emitter saturation voltage; typical values



T_j = 25 °C

Fig. 11. DC current gain as a function of collector current; typical values



V_{IM} = - 6 to + 8 V; V_{CC} = 250 V; t_p = 20 µs;
δ = t_p / T = 0.01
R_B and R_L calculated from I_{Con} and I_{Bon} requirements.

Fig. 12. Test circuit for resistive load switching

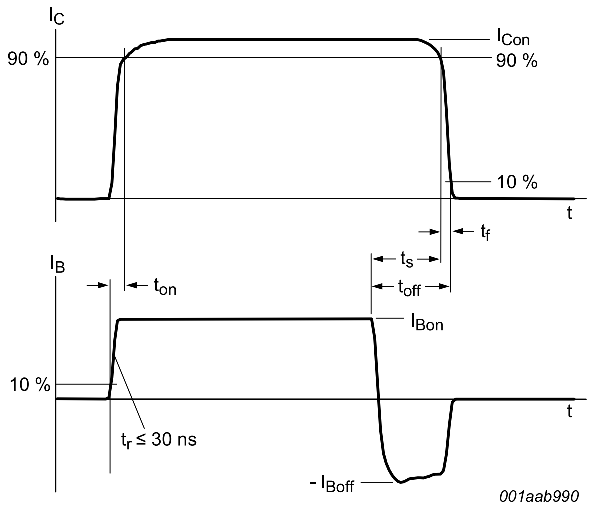
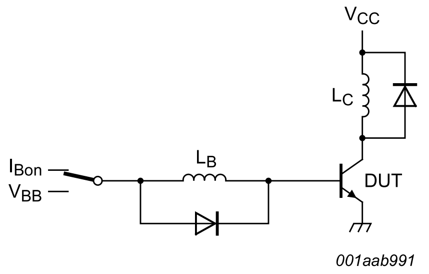


Fig. 13. Switching times waveforms for resistive load



V_{CC} = 300 V; V_{BB} = - 5 V; L_C = 200 µH; L_B = 1 µH

Fig. 14. Test circuit for inductive load switching

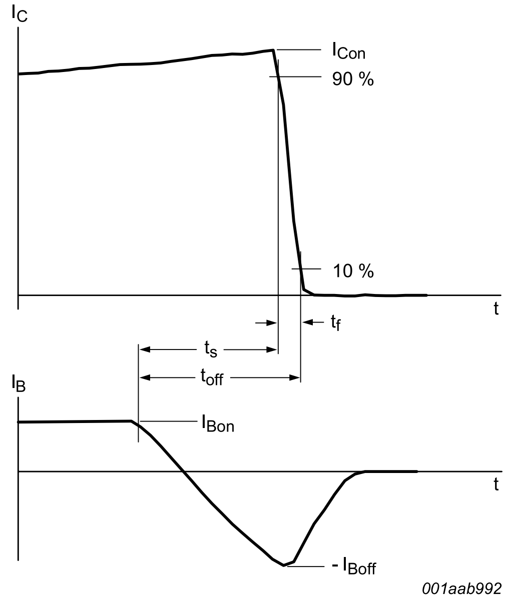
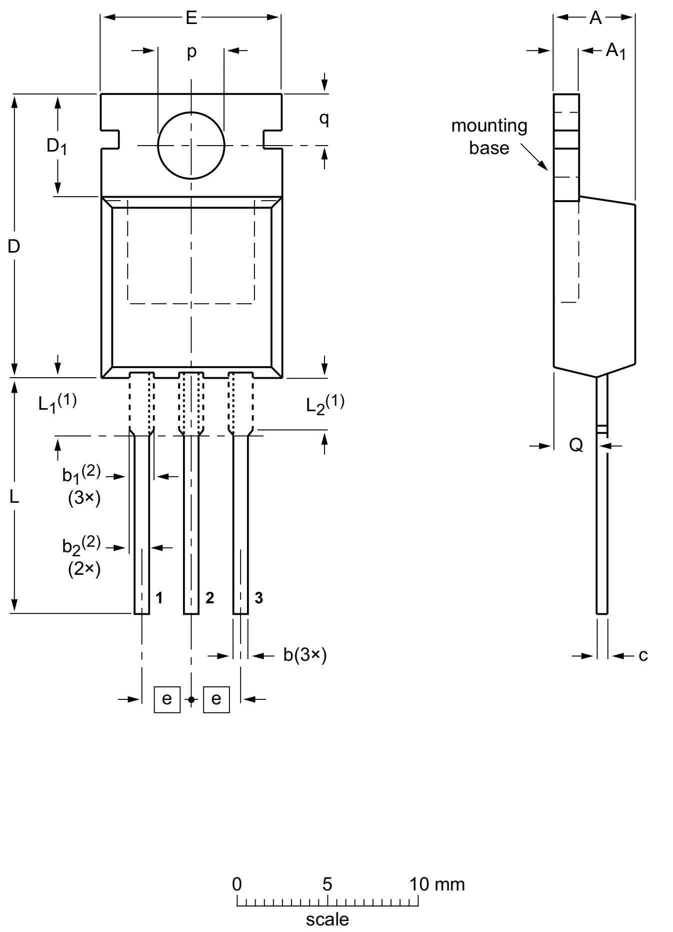


Fig. 15. Switching times waveforms for inductive load

10. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1(2)	b_2(2)	c	D	D_1	E	e	L	L_1(1)	L_2(1) max.	p	q	Q
mm	4.7 4.1	1.40 1.25	0.9 0.6	1.6 1.0	1.3 1.0	0.7 0.4	16.0 15.2	6.6 5.9	10.3 9.7	2.54	15.0 12.8	3.30 2.79	3.0	3.8 3.5	3.0 2.7	2.6 2.2

Notes

1. Lead shoulder designs may vary.
2. Dimension includes excess dambar.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT78		3-lead TO-220AB	SC-46			~~08-04-23~~ 08-06-13

11. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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