Features

ÿ Fully compatible with “ISO 11898” standard;

ÿ Built-in over-temperature protection function;

ÿ Bus port ±70V withstand voltage;

ÿ Driver (TXD) explicit timeout function;

ÿ Silent receiving mode;

ÿ SIT1051AT/E has a low power shutdown mode;

ÿ SIT1051AT/3 I/O voltage range supports 3.3V and 5V MCUs;

ÿ VCC and VIO power pins have undervoltage protection function;

ÿ High-speed CAN, supporting 5Mbps CAN FD flexible data rate;

ÿ The typical loop delay from TXD to RXD is less than 100ns;

ÿ High anti-electromagnetic interference capability;

ÿ Unpowered nodes do not interfere with the bus;

ÿ Support DFN3*3-8, small form factor, leadless package.

Product appearance diagram

Provide green and environmentally friendly lead-free packaging

describe

SIT1051A is an interface chip used between CAN protocol controller and physical bus, which can be used in trucks, public transportation, etc.

It supports 5Mbps flexible data rate CAN FD and has the advantages of bus and CAN protocol.

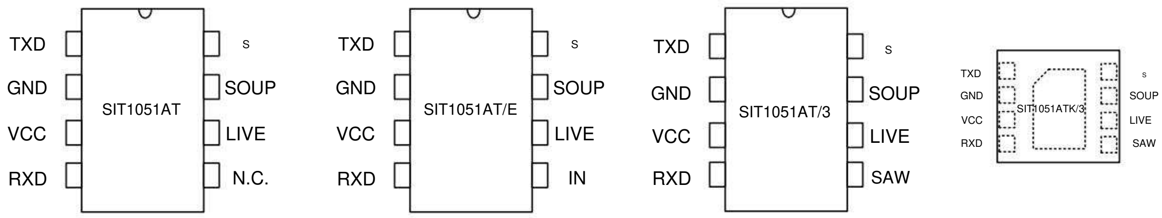
The ability to transmit differential signals between controllers.

SIT1051A is an upgraded version of SIT1051 chip, which improves the symmetry of bus signal and has lower electromagnetic radiation.

In addition, SIT1051A is fully compatible with SIT1051.

parameter	symbol	Test conditions	Minimum and	maximum units	
Supply voltage	VCC		4.5	5.5	In
Maximum transfer rate	1/tbit	NRZ	5		Mbaud
SOAKÿSOAK Pin voltage	Vcan		-70	+70	In
Bus differential voltage	Vdiff		1.5	3.0	In
Junction temperature	Tj		-40	150 ÿ	

Pinout



Pin Definition

Pin No.	Pin Name	Pin Function
1	TXD	Transmitter data input terminal
2	GND	Ground
3	VCC	Power Supply
4	RXD	Receiver data output
5	N.C.	No connection (SIT1051AT model)
5	VIO	Transceiver I/O level shifting supply voltage (SIT1051AT/3 models)
5	IN	Shutdown mode enable pin, low level is shutdown mode (SIT1051AT/E model)
6	CANL	Low potential CAN voltage input and output terminal
7	CANH	High potential CAN voltage input and output terminal
8	S	High-speed mode and silent mode selection, low level is high-speed mode

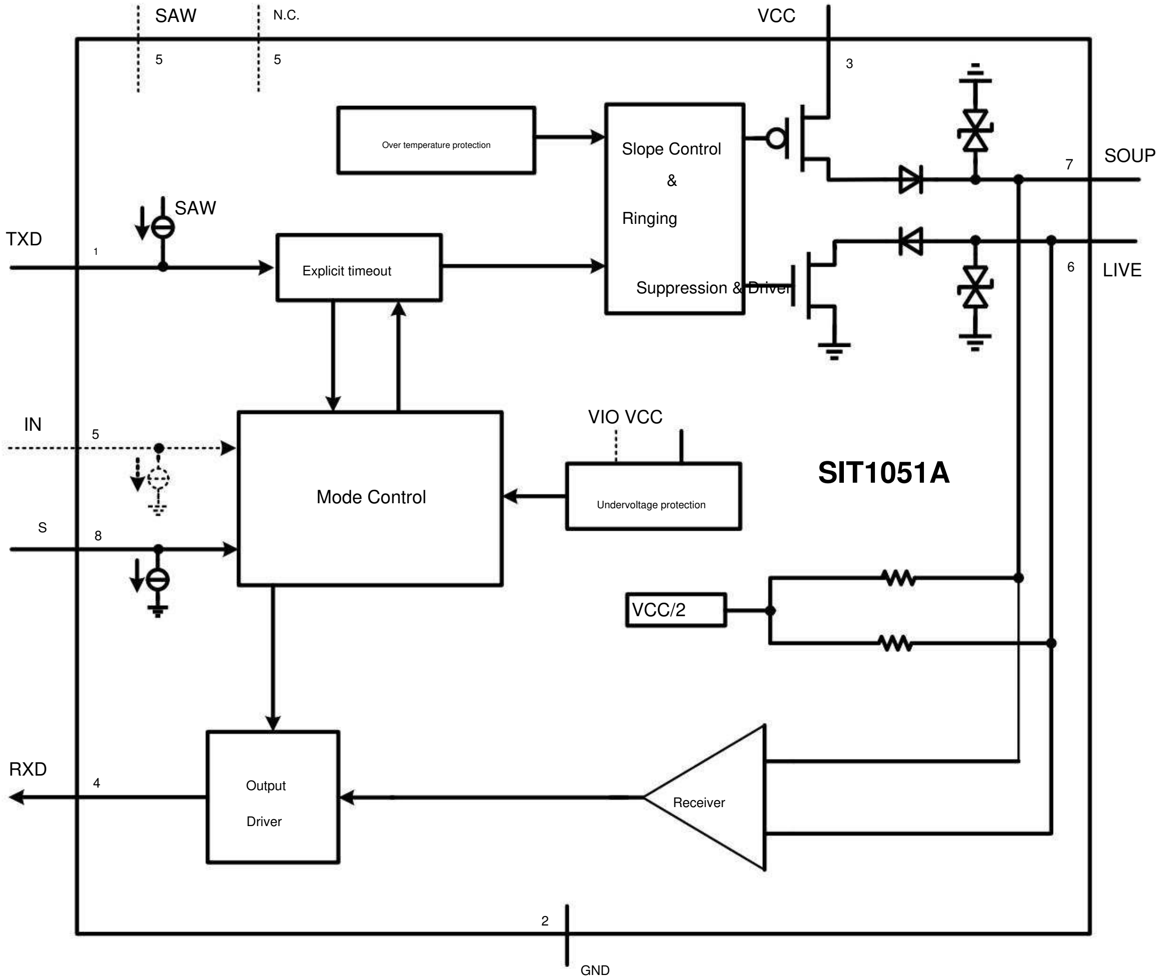
Limit parameters

parameter	symbol	size	unit
Supply voltage	VCC	-0.3~7	In
MCU side port	TXD, RXD, S, IN, VIO	-0.3~7	In
Bus side input voltage	CANL, CANLING	-70~70	In
Bus differential withstand voltage	VCANH-CANL	-27~27	In
Storage temperature range	Test	-55~150	ÿ
Junction temperature	Tj	-40~150	ÿ

The maximum limit parameter values refer to the values that may cause irreversible damage to the device if they are exceeded. Under these conditions, it is not conducive to the normal operation of the device.

Continuous operation of the device at the maximum allowable ratings may affect device reliability. All voltages are referenced to ground.

Internal circuit structure diagram



Bus Transmitter DC Characteristics

parameter	symbol	Test conditions	Min.	Typ.	Max.	Unit
CANH Output Voltage (Explicit)	VOH(D)	normal mode, TXD=0Vÿ RL=50ÿ to 65ÿ	2.75	3.5	4.5	In
CANL output voltage (Explicit)	VOL(D)		0.5	1.5	2.25	In
Bus output differential voltage (Explicit)	VOD(D)	Normal mode, TXD=0Vÿ RL=50ÿ to 65ÿ	1.5		3	In
		Normal mode, TXD=0Vÿ RL=45ÿ to 70ÿ	1.4		3.3	In
		Normal mode, TXD=0Vÿ RL=2240ÿ	1.5		5	In
Bus output voltage (implicit)	VO(R)	Normal mode, TXD=VIOÿ No load	2	0.5VCC	3	In
Bus differential output voltage (implicit)	VOD(R)	Normal mode, TXD=VIOÿ No load	-500		50	mV
Dominant output voltage symmetry	Vdom(TX)sym	Vdom(TX)sym=VCC- WATER - WATER	-400		400	mV
Output voltage symmetry	VTXsym	VTXsym= CANH + LIVEÿ RL=60ÿÿ CSPLIT=4.7nFÿ fTXD=250kHZÿ 1MHzÿ2MHz Figure 5	0.9VCC		1.1VCC	V
Dominant Implicit Common Mode Output voltage difference	Vcm(step)	Figure 3, Figure 5	-150		150	mV
dominant recessive common mode Peak-to-Peak	Vcm(p-p)	Figure 3, Figure 5	-300		300	mV
Dominant short circuit output current	IO(SC)DOM	Normal mode, TXD=0Vÿ CANH= -15V to 40V	-100	-70	-40	mA

parameter	symbol	Test conditions	Min.Typ.Max.Unit			
		Normal mode, TXD=0Vÿ LIVE= -15V to 40V	40	70	100 mA	
Recessive short-circuit output current IO(SC)REC		Normal mode, TXD=VIOÿ CANH=CANL= -27V to 32V	-3		3	m.a.

Unless otherwise specified, all typical values are measured at 25°C, power supply voltage VCC=5V, VIO=5V (if applicable), RL=60ÿ.

Bus Transmitter Switching Characteristics

parameter	symbol	Test Conditions Min Typ Max Unit				
Propagation delay (low to High)	td(TXD-busdom)	Normal mode, Figure 1, Figure 4		45		ns
Propagation Delay (High to Low)	td(TXD-busrec)	Normal mode, Figure 1, Figure 4		55		ns
Differential output rise time tr(BUS)				45		ns
Differential output fall time tf(BUS)				45		ns

Unless otherwise specified, all typical values are measured at 25°C, power supply voltage VCC=5V, VIO=5V (if applicable), RL=60ÿ.

Bus Receiver DC Characteristics

parameter	symbol	Test conditions	Min.Typ.Max.Unit			
Receiver threshold voltage Vth(RX)dif		Normal mode and Silent mode, -30V<VCM< 30V	0.5		0.9	In
Receiver Threshold Voltage Hysteresis range	Vhys(RX)dif	Normal mode and Silent mode, -30V<VCM< 30V	50	120	400 mV	
Receiver recessive voltage range Vrec(RX)		Normal mode and Silent mode, -30V<VCM< 30V	-3		0.5	In
Receiver dominant voltage range Vdom(RX)		Normal mode and Silent mode, -30V<VCM< 30V	0.9		8	In

parameter	symbol	Test conditions	Min.Typ.Max	Unit		
Bus leakage current	THE	VCC=VIO=0Vÿ CANH= LIVE=5V	-10		10	ÿA
CANH, CANL input resistance	ALSO	-2VÿCANHÿ7V -2VÿCANLÿ7V	9	15	28	kÿ
CANH, CANL differential Input resistance	RID	-2VÿCANHÿ7V -2VÿCANLÿ7V	19	30	52	kÿ
CANH, CANL input Resistor Mismatch	ÿRIN	0VÿCANHÿ5V 0VÿCANLÿ5V	-2		2	%
CANH, CANL to ground Input Capacitance	BIN	TXD=VIO		24		pF
CANH, CANL differential Input Capacitance	CID	TXD=VIO		12		pF
Bus slew rate	SR	Bus differential voltage display Sexuality to the edge of invisibility			70	V/ÿs

Unless otherwise specified, all typical values are measured at 25°C, power supply voltage VCC=5V, VIO=5V (if applicable), RL=60ÿ.

Bus Receiver Switching Characteristics

parameter	symbol	Test conditions	Min.Typ.Max	Unit		
Propagation Delay (Low to High)	td(busdom- RXD)	Normal mode, Figure 1, Figure 4		45		ns
Propagation Delay (High to Low)	td(busrec- RXD)	Normal mode, Figure 1, Figure 4		45		ns
RXD signal rise time tr(RXD)				8		ns
RXD signal fall time tf(RXD)				8		ns

Unless otherwise specified, all typical values are measured at 25°C, power supply voltage VCC=5V, VIO=5V (if applicable), RL=60ÿ.

Device switching characteristics

parameter	Symbol Test	Conditions Min Typ Max Units				
Loop delay 1, TXD down Falling edge to RXD falling	tloop1	Normal mode, Figure 1, Figure 4	40		160	ns
edge loop delay 2, TXD up Rising edge to RXD rising edge	tloop2	Normal mode, Figure 1, Figure 4	40		175	ns
BUS output bit time tbit(BUS)		tbit(TXD)=500ns	435		530	ns

parameter	Symbol	Test Conditions	Min	Typ	Max	Units
		tbit(TXD)=200ns	155		210	ns
RXD output bit time	tbit(RXD)	tbit(TXD)=500ns	400		550	ns
		tbit(TXD)=200ns	120		220	ns
BUS and RXD output Bit time difference	ÿtrec	ÿtrec= tbit(RXD)- tbit(BUS)ÿ tbit(TXD)=500ns	-65		40	ns
		ÿtrec= tbit(RXD)- tbit(BUS)ÿ tbit(TXD)=200ns	-45		15	ns
TXD dominant timeout time	tdom_TXD		0.8	2	4	ms

Unless otherwise specified, all typical values are measured at 25°C, power supply voltage VCC=5V, VIO=5V (if applicable), RL=60ÿ.

TXD Pin Characteristics

parameter	symbol	Test Conditions	Min	Typ	Max	Unit
TXD port high level input Incoming current	IIH(TXD)	TXD=VIO	-5		5	ÿA
TXD port low level input Incoming current	IIL(TXD)	TXD=0V	-260	-150	-30	ÿA
Unpowered TXD leakage current	IO(off)	VCC=VIO=0Vÿ TXD=5.5V	-1		1	ÿA
Input high level lower limit	VIH	SIT1051AT/3	0.7VIO(1)		VIO+0.3	V
Input low level upper limit	VIL	SIT1051AT/3	-0.3		0.3VIO	In
Input high level lower limit	VIH	SIT1051AT	2		VCC+0.3	V
Input low level upper limit	VIL	SIT1051AT	-0.3		0.8	In
TXD port floating voltage	TXDO			H		logic

(1) SIT1051AT/E model VIO=VCC;

Unless otherwise specified, all typical values are measured at 25°C, power supply voltage VCC=5V, VIO=5V (if applicable), RL=60ÿ.

S Pin Characteristics

parameter	Symbol	Test Conditions	Min	Typ	Max	Units
S port high level input current	IIH(S)	S=VIO	1		10	ÿA
S port low level input current	IIL(S)	S=0V	-1		1	ÿA

parameter	Symbol Test Conditions Min Typ Max Units					
No power S leakage current IO(off)		VCC=VIO=0Vÿ S=5.5V	-1		1	ÿA
Input high level lower limit VIH		SIT1051AT/3	0.7VIO (1)		VIO+0.3 V	
Input low level upper limit VIL		SIT1051AT/3	-0.3		0.3VIO	In
Input high level lower limit VIH		SIT1051AT	2		VCC+0.3 V	
Input low level upper limit VIL		SIT1051AT	-0.3		0.8	In
S port floating voltage	SO		L			logic

(1) SIT1051AT/E model VIO=VCC;

Unless otherwise specified, all typical values are measured at 25°C, power supply voltage VCC=5V, VIO=5V (if applicable), RL=60ÿ.

EN Pin Characteristics

parameter	symbol	Test Conditions Min Typ Max Unit				
EN port high level input Current	IIH(EN)	EN=VCC	1		10	ÿA
EN port low level input	IIL(EN)	EN=0V	-1		1	ÿA
Current input high level lower limit VIH			0.7VCC		VCC+0.3 V	
Input low level upper limit VIL			-0.3		0.3VCC V	
EN leakage current IO(off) when power is not on		VCC=0Vÿ EN=5.5V	-1		1	ÿA
EN port floating voltage ENO			L			logic

Unless otherwise specified, all typical values are measured at 25°C, power supply voltage VCC=5V, VIO=5V (if applicable), RL=60ÿ.

RXD Pin Characteristics

parameter	symbol	Test Conditions Min Typ Max Unit				
RXD port high level input Output current	IOH(RXD)	VIO=VCCÿ RXD=VIO-0.4V	-8	-3	-1	m.a.
RXD port low level input Output current	IOL(RXD)	RXD=0.4Vÿ Bus Dominant	2	5	12	m.a.
Unpowered RXD leakage current IO(off)		VCC=VIO=0Vÿ RXD=5.5V	-1		1	ÿA

Unless otherwise specified, all typical values are measured at 25°C, power supply voltage VCC=5V, VIO=5V (if applicable), RL=60ÿ.

Supply current

parameter	symbol	Test conditions	Min.	Typ.	Max.	Unit
VCC Supply Current	ICC_D	Normal Mode Dominant		45	70	mA
	ICC_R	Normal Mode Recessive		5	10	mA
	ICC_S	Silent Mode		1.5	3	m.a.
	ICC_OFF	Shutdown Mode (Model SIT1051AT/E)		5	8	ÿA
VIO supply current	IIO_D	TXD=0V		170	300	ÿA
	IIO_R	TXD=VIO		15	30	ÿA

Unless otherwise specified, all typical values are measured at 25°C, power supply voltage VCC=5V, VIO=5V (if applicable), RL=60ÿ.

Over temperature protection

parameter	symbol	Test Conditions	Min	Typ	Max	Unit
Over temperature shutdown	Tj(sd)			190		ÿ

Unless otherwise specified, all typical values are measured at 25°C, power supply voltage VCC=5V, VIO=5V (if applicable), RL=60ÿ.

Undervoltage protection

parameter	symbol	Test Conditions	Min	Typ	Max	Unit
VCC undervoltage protection	Vuvd_VCC		3.7	4	4.3	In
VIO undervoltage protection	Vuvd_VIO		1.7	2	2.3	In

Unless otherwise specified, all typical values are measured at 25°C, power supply voltage VCC = 5V, VIO = 5V (if applicable), RL = 60ÿ.

ESD Performance

parameter	symbol	Test Conditions	Min	Typ	Max	Unit
CAN bus pin contacts Discharge model (IEC)	VESD_IEC	IEC 61000-4-2: Contact discharge (SOUP, (LIVE)	-4		+4	kV

parameter	symbol	Test Conditions Min Typ Max Unit				
Human body discharge model ÿHBMÿ	VESD_HBM all ports		-8		+8	kV
Component Charging Model ÿCDMÿ	VESD_CDM		-750		+750	In
Mechanical Model (MM) VESD_MM			-300		+300	In

Function Table

Table 1 CAN transceiver truth table

TXD(1)	S (1)	COFFEE(1)	LIVE(1)	BUS Status RXD(1)	
L	L (or floating)	H	L	Dominant	L
H (or floating null)	L (or floating) 0.5VCC		0.5VCC	Hidden	H
X	H	0.5VCC	0.5VCC	Hidden	H

(1) H = high level; L = low level; X = don't care.

Table 2 Receiver Function Table

VID=CANH-CANL	BUS status	RXD(1)
VIDÿ0.9V	dominant	L
0.5< VID<0.9V	?	?
VIDÿ0.5V	Hidden	H

(1) H = high level; L = low level; ? = uncertain.

Table 3 Undervoltage protection status table

VCC	SAW(1)	BUS status BUS output (2) normal		RXD(2)
VCC>Vuvd_VCC	VIO>Vuvd_VIO		Follow the bus according to S and TXD	
VCC<Vuvd_VCC	VIO>Vuvd_VIO	Protected State	WITH	H
VCC>Vuvd_VCC	VIO<Vuvd_VIO	Protected State	WITH	H
VCC<Vuvd_VCC	VIO<Vuvd_VIO	Protected State	WITH	H

(1) Model SIT1051AT/3 and Model SIT1051ATK/3;

(2) H = high level; Z = high impedance state.

Waveform timing diagram

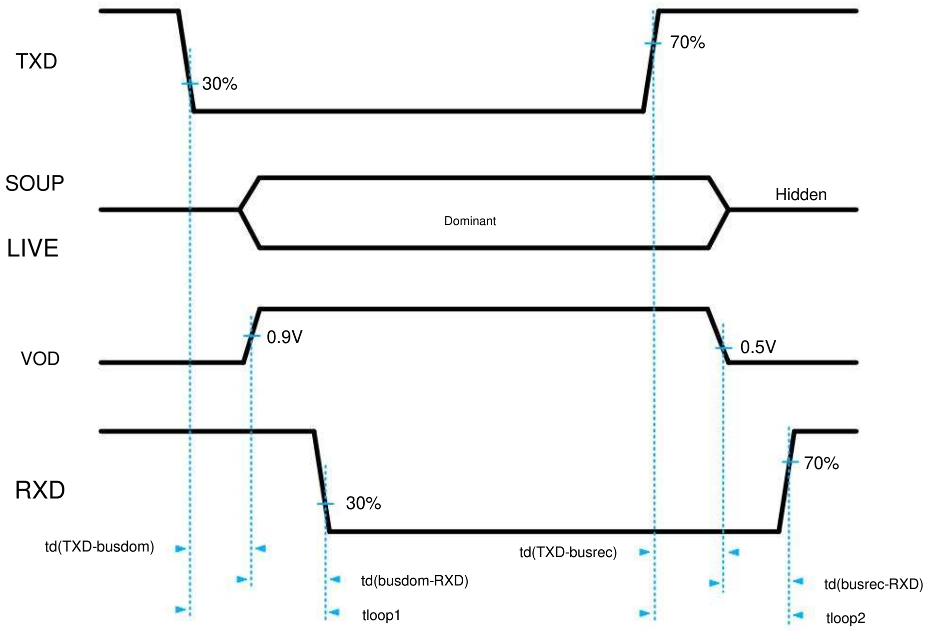


Figure **1** Transceiver transmission delay diagram

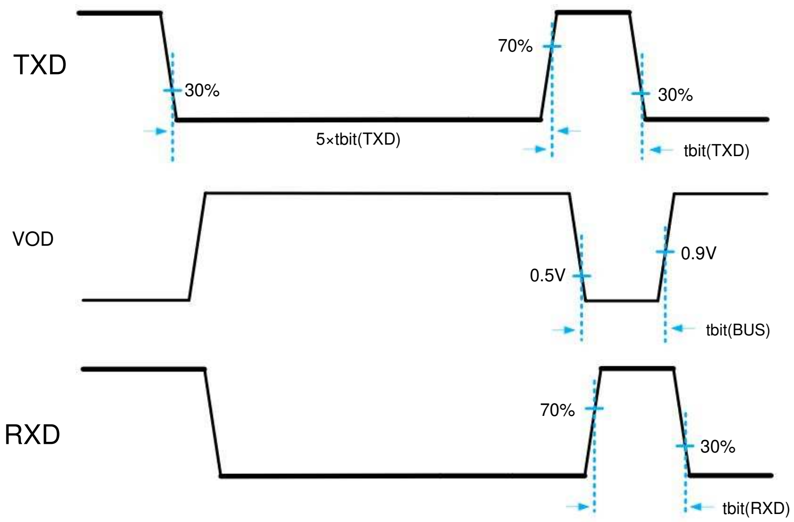


Figure **2** tbit delay diagram

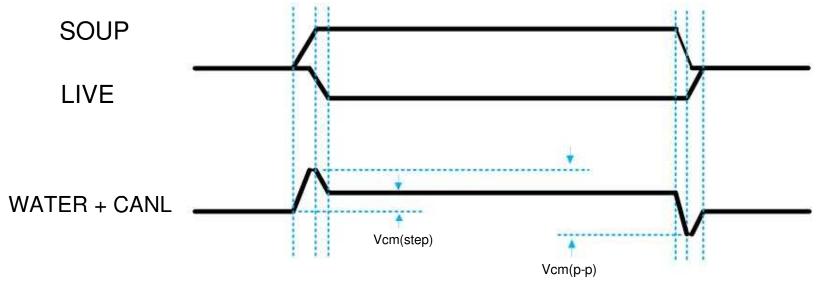


Figure **3** Bus common mode voltage (SAE **1939-14)**

Test Circuit

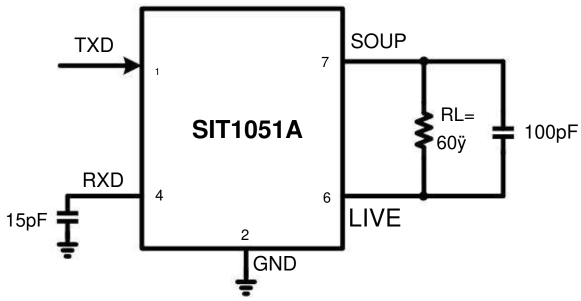


Figure **4** Transceiver timing test circuit diagram

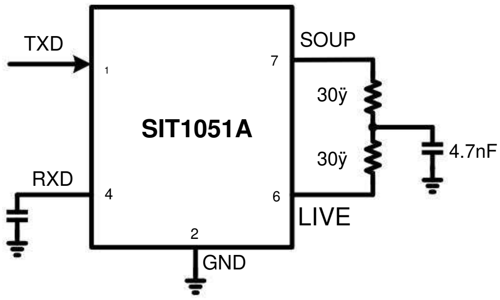


Figure **5** Transceiver bus symmetry test circuit diagram

Typical application diagram

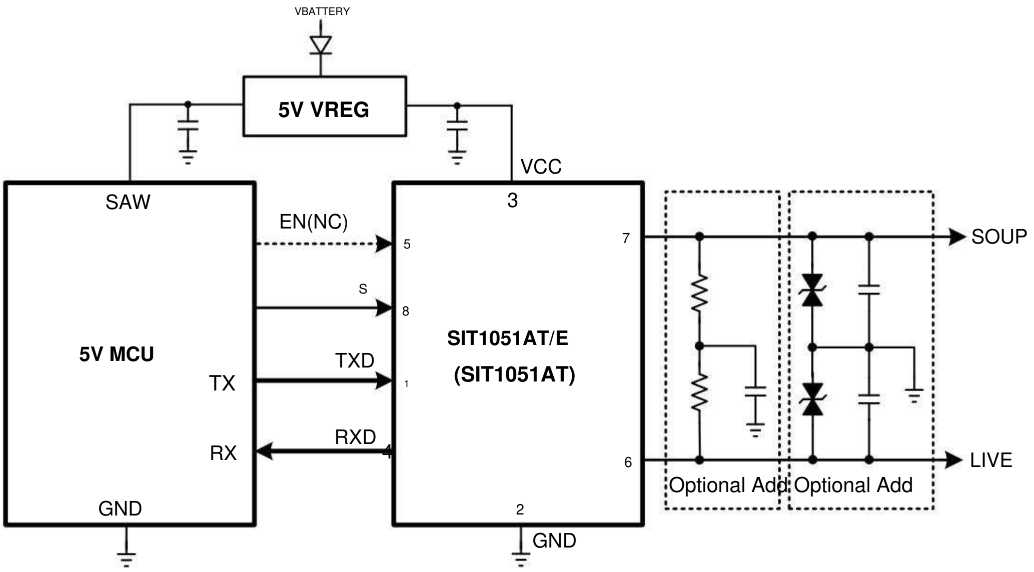


Figure 6 Typical application diagram of **SIT1051AT/E (or SIT1051AT) and 5V MCU**

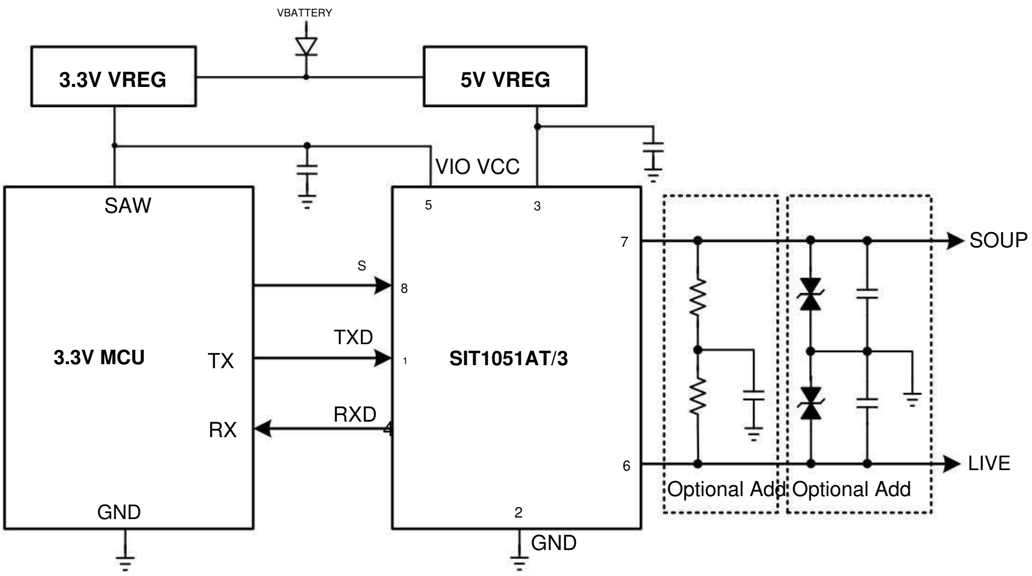


Figure 7 Typical application diagram of **SIT1051AT/3** and **3.3V MCU**

illustrate

1Brief

Description SIT1051A is an interface chip used between CAN protocol controller and physical bus. It can be used in trucks, buses, cars, industrial control and other fields. It supports 5Mbps flexible data rate CAN FD and has the ability to transmit differential signals between the bus and CAN protocol controller. It is fully compatible with the "ISO 11898" standard.

2Short circuit protection

The driver stage of SIT1051A has a current limiting protection function to prevent the driver circuit from being short-circuited to the positive and negative power supply voltages.

The power consumption will increase, and the short-circuit protection function can protect the driver stage from being damaged.

3Over temperature protection

SIT1051A has an over-temperature protection function. After the over-temperature protection is triggered, the current of the driver stage will decrease because the driver tube is the main power consumption.

For energy-saving components, the current reduction can reduce power consumption and thus reduce chip temperature. At the same time, other parts of the chip still maintain normal operation.

4 Undervoltage

Protection SIT1051A has an undervoltage detection function on the power pin, which can put the device into a protected mode.

The bus is protected (bus output high impedance) when Vuvd_VCC or VIO is lower than Vuvd_VIO (if applicable).

5 Control Modes

The control pin S allows selection of two operating modes: high speed mode and silent mode.

High-speed mode is the normal operating mode and is selected by grounding or floating pin S. Both the CAN driver and receiver can

Fully operational and CAN communication is bidirectional.

Silent mode is activated by setting pin S high. The CAN driver is switched off, but the receiver continues to operate.

6 Dominant timeout function

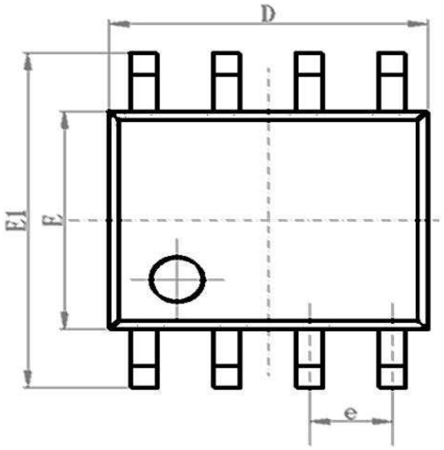
In high-speed mode, if the low level on pin TXD lasts longer than the internal timer value (tdom_TXD), the transmitter will be disabled and drive the bus into the recessive state. This prevents pin TXD from being forced to a permanent low level due to hardware or software application failures.

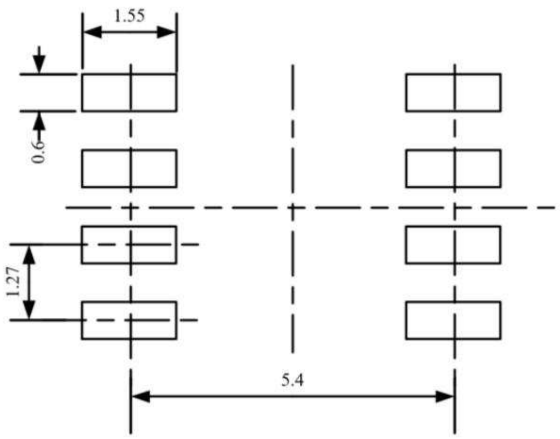
The bus line is driven to a permanent dominant state (blocking all network communication). A rising edge on pin TXD resets it.

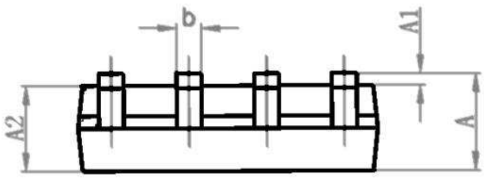
SOP8 dimensions

Package size

Symbol	**Minimum value/mm**	**Typical value/mm**	**Maximum value/mm**
A	1.40	·	1.80
A1	0.10	·	0.25
A2	1.30	1.40	1.50
b	0.38	·	0.51
D	4.80	4.90	5.00
AND	3.80	3.90	4.00
E1	5.80	6.00	6.20
and		1.27BSC	
L	0.40	0.60	0.80
c	0.20	·	0.25
i	0°	·	8°





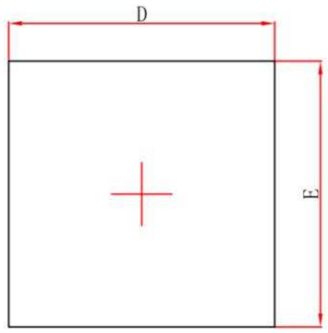


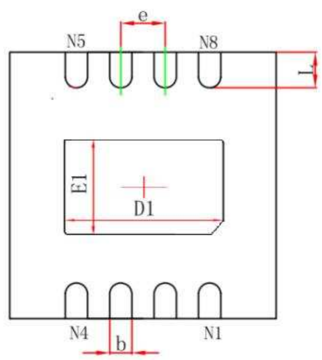
LAND PATTERN EXAMPLE (Unit: mm)

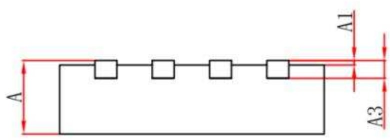
DFN3*3-8 dimensions

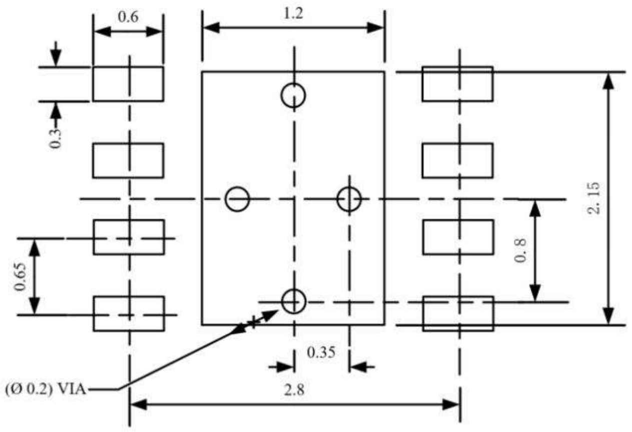
Package size

Symbol	Minimum value/mm	Typical value/mm	Maximum value/mm
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.203 REF		
D	2.90	3.00	3.10
AND	2.90	3.00	3.10
D1	2.05	2.15	2.25
E1	1.10	1.20	1.30
b	0.25	0.30	0.35
and	0.65 TYPE		
L	0.35	0.4	0.45



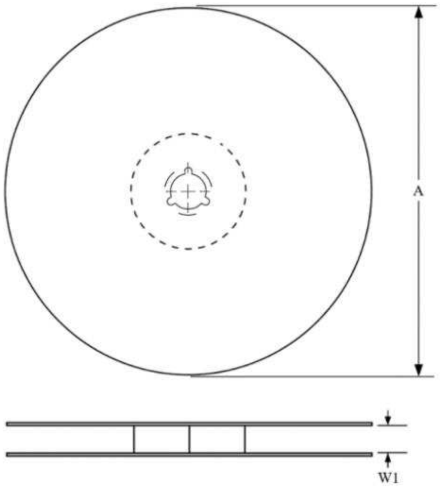




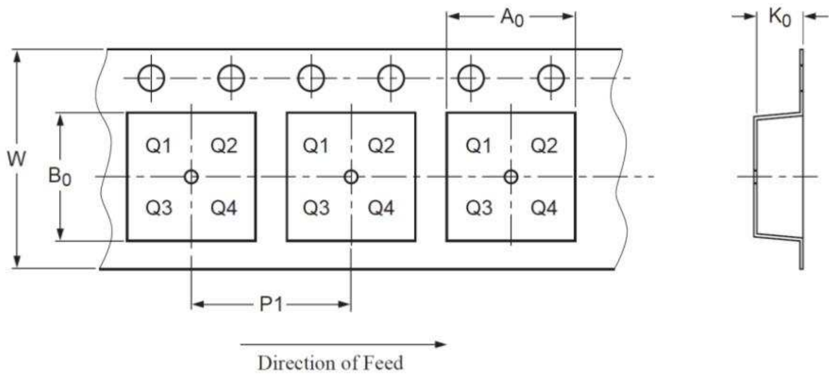


LAND PATTERN EXAMPLE (Unit: mm)

Taping Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



PIN1 is in quadrant 1

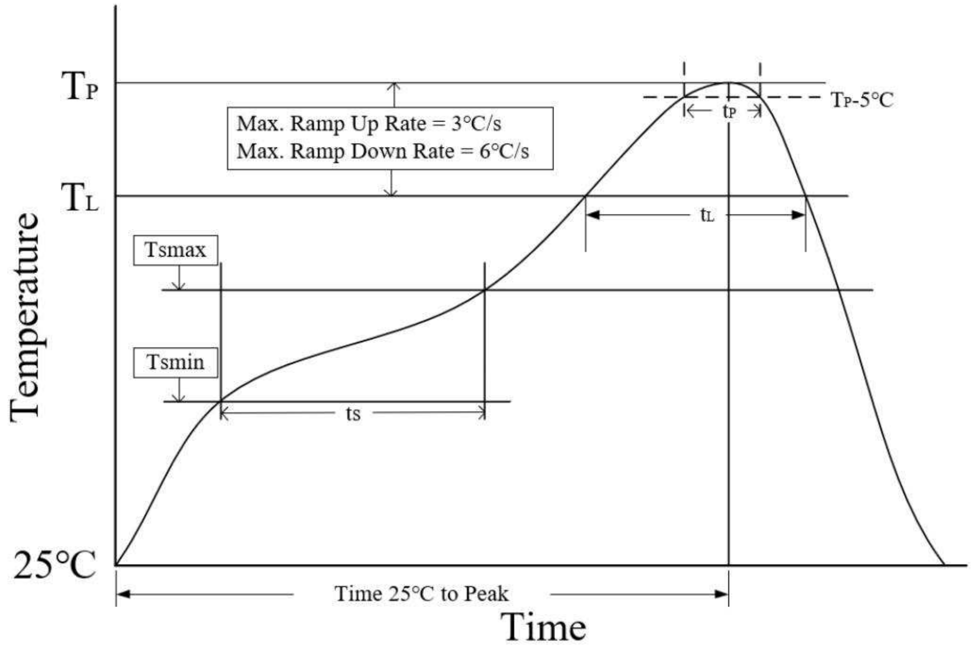
Package Type	Reel diameter A (mm)	Tape width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	IN (mm)
SOP8	330ÿ1	12.4	6.60ÿ0.1	5.30ÿ0.10	1.90ÿ0.1	8.00ÿ0.1	12.00ÿ0.1
DFN3*3-8	329ÿ1	12.4	3.30ÿ0.1	3.30ÿ0.1	1.10ÿ0.1	8.00ÿ0.1	12.00ÿ0.3

Ordering Information

Order code	Encapsulation	Packaging
SIT1051AT	SOP8	Tape
SIT1051AT/E	SOP8	Tape
SIT1051AT/3	SOP8	Tape
SIT1051ATK/3	DFN3*3-8, small form factor, no pins	Tape

SOP8 taping and packaging is 2500 pieces/reel, DFN3*3-8 taping and packaging is 6000 pieces/reel.

Reflow



	Lead-free soldering conditions
Parameters Average temperature rise	3 ÿ/second max
rate (TL to TP) Preheating time ts (Tsmin = 150 ÿ to Tsmax =	60-120 seconds
200 ÿ) Tin melting time tL (TL = 217	60-150 seconds
ÿ) Peak	260-265 ÿ
temperature TP is less than the peak	30 seconds
temperature within 5 ÿ tP Average	6 ÿ/second max
cooling rate (TP to TL) Normal temperature 25ÿ to peak temperature TP time	8 minutes max

Important Notice

Xinlite reserves the right to change the above information without prior notice.

Revision History

Version Number	Revisions	Revision time
V1.0	Initial version.	2022.10