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## Hex Schmitt-Trigger Inverter High-Performance Silicon-Gate CMOS

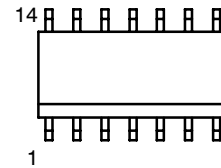
The 74HC14 is identical in pinout to the LS14, LS04 and the HC04. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC14 is useful to “square up” slow input rise and fall times. Due to hysteresis voltage of the Schmitt trigger, the HC14 finds applications in noisy environments.

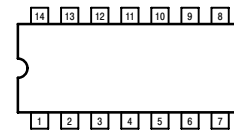
**Features**

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7A Requirements
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 60 FETs or 15 Equivalent Gates
- These are Pb-Free Devices

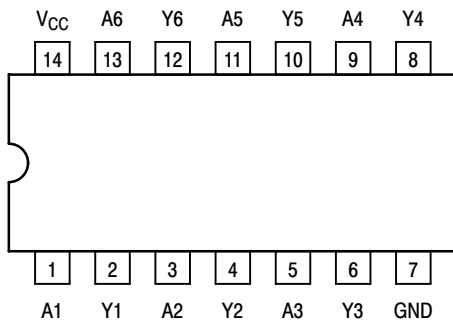
**SOP -14**



**DIP -14**



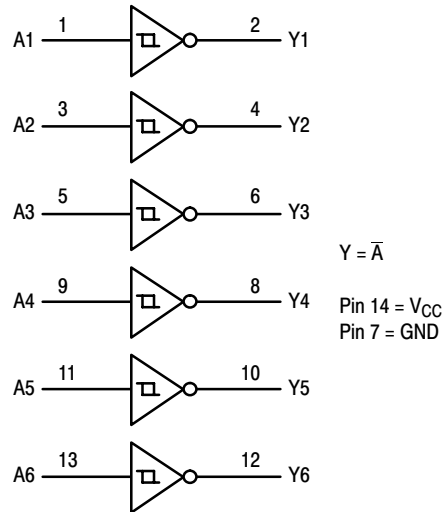
**Pinout: 14-Lead Packages (Top View)**



**FUNCTION TABLE**

| Inputs | Outputs |
|--------|---------|
| A      | Y       |
| L      | H       |
| H      | L       |

**LOGIC DIAGRAM**



### MAXIMUM RATINGS

| Symbol    | Parameter  | Value                   | Unit |
|-----------|--|-------------------------|------|
| $V_{CC}$  | DC Supply Voltage (Referenced to GND)                                    | - 0.5 to + 7.0          | V    |
| $V_{in}$  | DC Input Voltage (Referenced to GND)                                     | - 0.5 to $V_{CC} + 0.5$ | V    |
| $V_{out}$ | DC Output Voltage (Referenced to GND)                                    | - 0.5 to $V_{CC} + 0.5$ | V    |
| $I_{in}$  | DC Input Current, per Pin  | ±20                     | mA   |
| $I_{out}$ | DC Output Current, per Pin   | ±25                     | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins                                 | ±50                     | mA   |
| $P_D$     | Power Dissipation in Still Air, SOIC Package†<br>TSSOP Package†          | 500<br>450              | mW   |
| $T_{stg}$ | Storage Temperature Range  | - 65 to + 150           | °C   |
| $T_L$     | Lead Temperature, 1 mm from Case for 10 Seconds<br>SOIC or TSSOP Package | 260                     | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — SOIC Package: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

### RECOMMENDED OPERATING CONDITIONS

| Symbol            | Parameter  | Min  | Max       | Unit |
|-------------------|--|------|-----------|------|
| $V_{CC}$          | DC Supply Voltage (Referenced to GND)                | 2.0  | 6.0       | V    |
| $V_{in}, V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0    | $V_{CC}$  | V    |
| $T_A$             | Operating Temperature Range, All Package Types       | - 55 | + 125     | °C   |
| $t_r, t_f$        | Input Rise/Fall Time<br>(Figure 1)                   |      |           |      |
|                   | $V_{CC} = 2.0 \text{ V}$                             | 0    | No Limit* | ns   |
|                   | $V_{CC} = 4.5 \text{ V}$                             | 0    | No Limit* |      |
|                   | $V_{CC} = 6.0 \text{ V}$                             | 0    | No Limit* |      |

\*When  $V_{in} = 50\% V_{CC}$ ,  $I_{CC} > 1\text{mA}$

**DC CHARACTERISTICS** (Voltages Referenced to GND)

| Symbol                       | Parameter  | Condition  | V <sub>CC</sub><br>(V) | Guaranteed Limit |       |        | Unit |
|------------------------------|--|--|------------------------|------------------|-------|--------|------|
|                              |  |  |                        | -55 to 25°C      | ≤85°C | ≤125°C |      |
| V <sub>T+</sub> max          | Maximum Positive-Going Input Threshold Voltage<br>(Figure 3) | V <sub>out</sub> = 0.1V<br> I <sub>out</sub>   ≤ 20μA  | 2.0                    | 1.50             | 1.50  | 1.50   | V    |
|                              |  |  | 3.0                    | 2.15             | 2.15  | 2.15   |      |
|                              |  |  | 4.5                    | 3.15             | 3.15  | 3.15   |      |
|                              |  |  | 6.0                    | 4.20             | 4.20  | 4.20   |      |
| V <sub>T+</sub> min          | Minimum Positive-Going Input Threshold Voltage<br>(Figure 3) | V <sub>out</sub> = 0.1V<br> I <sub>out</sub>   ≤ 20μA  | 2.0                    | 1.0              | 0.95  | 0.95   | V    |
|                              |  |  | 3.0                    | 1.5              | 1.45  | 1.45   |      |
|                              |  |  | 4.5                    | 2.3              | 2.25  | 2.25   |      |
|                              |  |  | 6.0                    | 3.0              | 2.95  | 2.95   |      |
| V <sub>T-</sub> max          | Maximum Negative-Going Input Threshold Voltage<br>(Figure 3) | V <sub>out</sub> = V <sub>CC</sub> - 0.1V<br> I <sub>out</sub>   ≤ 20μA  | 2.0                    | 0.9              | 0.95  | 0.95   | V    |
|                              |  |  | 3.0                    | 1.4              | 1.45  | 1.45   |      |
|                              |  |  | 4.5                    | 2.0              | 2.05  | 2.05   |      |
|                              |  |  | 6.0                    | 2.6              | 2.65  | 2.65   |      |
| V <sub>T-</sub> min          | Minimum Negative-Going Input Threshold Voltage<br>(Figure 3) | V <sub>out</sub> = V <sub>CC</sub> - 0.1V<br> I <sub>out</sub>   ≤ 20μA  | 2.0                    | 0.3              | 0.3   | 0.3    | V    |
|                              |  |  | 3.0                    | 0.5              | 0.5   | 0.5    |      |
|                              |  |  | 4.5                    | 0.9              | 0.9   | 0.9    |      |
|                              |  |  | 6.0                    | 1.2              | 1.2   | 1.2    |      |
| V <sub>H</sub> max<br>Note 2 | Maximum Hysteresis Voltage<br>(Figure 3)                     | V <sub>out</sub> = 0.1V or V <sub>CC</sub> - 0.1V<br> I <sub>out</sub>   ≤ 20μA  | 2.0                    | 1.20             | 1.20  | 1.20   | V    |
|                              |  |  | 3.0                    | 1.65             | 1.65  | 1.65   |      |
|                              |  |  | 4.5                    | 2.25             | 2.25  | 2.25   |      |
|                              |  |  | 6.0                    | 3.00             | 3.00  | 3.00   |      |
| V <sub>H</sub> min<br>Note 2 | Minimum Hysteresis Voltage<br>(Figure 3)                     | V <sub>out</sub> = 0.1V or V <sub>CC</sub> - 0.1V<br> I <sub>out</sub>   ≤ 20μA  | 2.0                    | 0.20             | 0.20  | 0.20   | V    |
|                              |  |  | 3.0                    | 0.25             | 0.25  | 0.25   |      |
|                              |  |  | 4.5                    | 0.40             | 0.40  | 0.40   |      |
|                              |  |  | 6.0                    | 0.50             | 0.50  | 0.50   |      |
| V <sub>OH</sub>              | Minimum High-Level Output Voltage                            | V <sub>in</sub> ≤ V <sub>T-</sub> min<br> I <sub>out</sub>   ≤ 20μA  | 2.0                    | 1.9              | 1.9   | 1.9    | V    |
|                              |  |  | 4.5                    | 4.4              | 4.4   | 4.4    |      |
|                              |  | V <sub>in</sub> ≤ V <sub>T-</sub> min     I <sub>out</sub>   ≤ 2.4mA<br> I <sub>out</sub>   ≤ 4.0mA<br> I <sub>out</sub>   ≤ 5.2mA | 3.0                    | 2.48             | 2.34  | 2.20   |      |
|                              |  |  | 4.5                    | 3.98             | 3.84  | 3.70   |      |
| V <sub>OL</sub>              | Maximum Low-Level Output Voltage                             | V <sub>in</sub> ≥ V <sub>T+</sub> max<br> I <sub>out</sub>   ≤ 20μA  | 2.0                    | 0.1              | 0.1   | 0.1    | V    |
|                              |  |  | 4.5                    | 0.1              | 0.1   | 0.1    |      |
|                              |  | V <sub>in</sub> ≥ V <sub>T+</sub> max     I <sub>out</sub>   ≤ 2.4mA<br> I <sub>out</sub>   ≤ 4.0mA<br> I <sub>out</sub>   ≤ 5.2mA | 3.0                    | 0.26             | 0.33  | 0.40   |      |
|                              |  |  | 4.5                    | 0.26             | 0.33  | 0.40   |      |
| I <sub>in</sub>              | Maximum Input Leakage Current                                | V <sub>in</sub> = V <sub>CC</sub> or GND   | 6.0                    | ±0.1             | ±1.0  | ±1.0   | μA   |
| I <sub>CC</sub>              | Maximum Quiescent Supply Current (per Package)               | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0μA   | 6.0                    | 2.0              | 20    | 40     | μA   |

- Information on typical parametric values along with frequency or heavy load considerations can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).
- V<sub>H</sub>min > (V<sub>T+</sub> min) - (V<sub>T-</sub> max); V<sub>H</sub>max = (V<sub>T+</sub> max) - (V<sub>T-</sub> min).

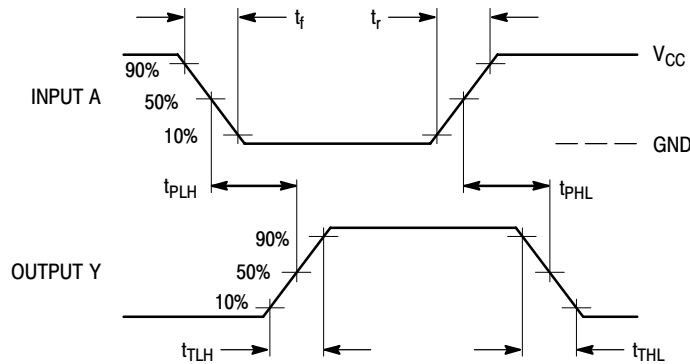
**AC CHARACTERISTICS** ( $C_L = 50\text{pF}$ , Input  $t_r = t_f = 6\text{ns}$ )

| Symbol                   | Parameter  | $V_{CC}$<br>(V) | Guaranteed Limit |       |        | Unit |
|--------------------------|--|-----------------|------------------|-------|--------|------|
|                          |  |                 | -55 to 25°C      | ≤85°C | ≤125°C |      |
| $t_{PLH}$ ,<br>$t_{PHL}$ | Maximum Propagation Delay, Input A or B to Output Y<br>(Figures 1 and 2) | 2.0             | 75               | 95    | 110    | ns   |
|                          |  | 3.0             | 30               | 40    | 55     |      |
|                          |  | 4.5             | 15               | 19    | 22     |      |
|                          |  | 6.0             | 13               | 16    | 19     |      |
| $t_{TLH}$ ,<br>$t_{THL}$ | Maximum Output Transition Time, Any Output<br>(Figures 1 and 2)          | 2.0             | 75               | 95    | 110    | ns   |
|                          |  | 3.0             | 27               | 32    | 36     |      |
|                          |  | 4.5             | 15               | 19    | 22     |      |
|                          |  | 6.0             | 13               | 16    | 19     |      |
| $C_{in}$                 | Maximum Input Capacitance  |                 | 10               | 10    | 10     | pF   |

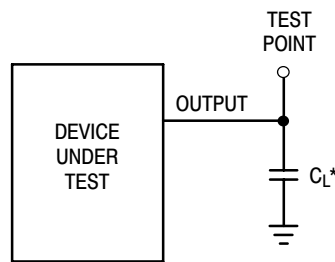
NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

| $C_{PD}$ | Power Dissipation Capacitance (Per Inverter)* | Typical @ 25°C, $V_{CC} = 5.0\text{ V}$ |  | pF |
|----------|---|---|--|----|
|          |   | 22                                      |  |    |
|          |   |   |  |    |

\*Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ . For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

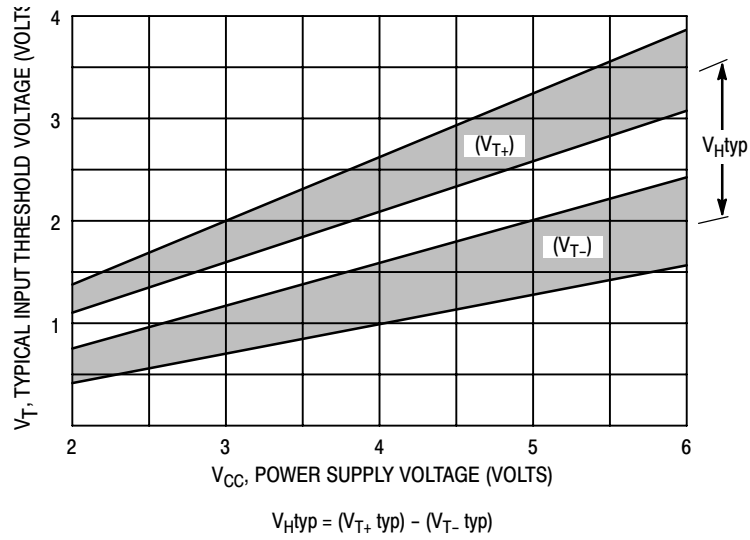


**Figure 1. Switching Waveforms**

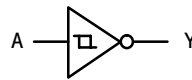


\*Includes all probe and jig capacitance

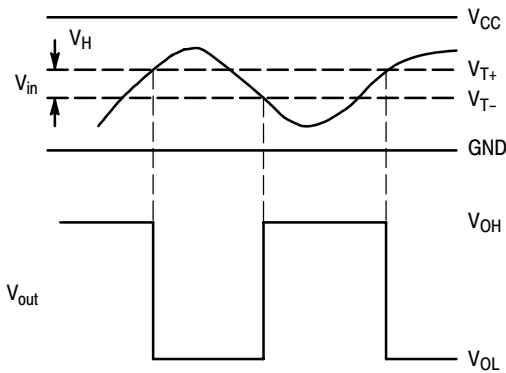
**Figure 2. Test Circuit**



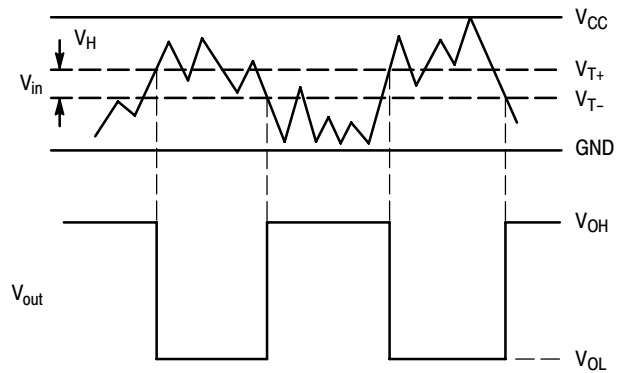
**Figure 3. Typical Input Threshold,  $V_{T+}$ ,  $V_{T-}$  versus Power Supply Voltage**



(a) A Schmitt-Trigger Squares Up Inputs With Slow Rise and Fall Times



(b) A Schmitt-Trigger Offers Maximum Noise Immunity



**Figure 4. Typical Schmitt-Trigger Applications**